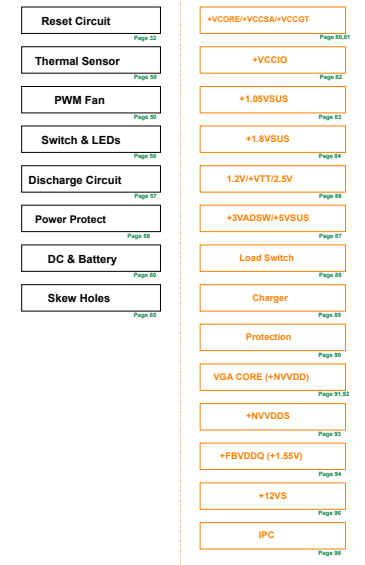
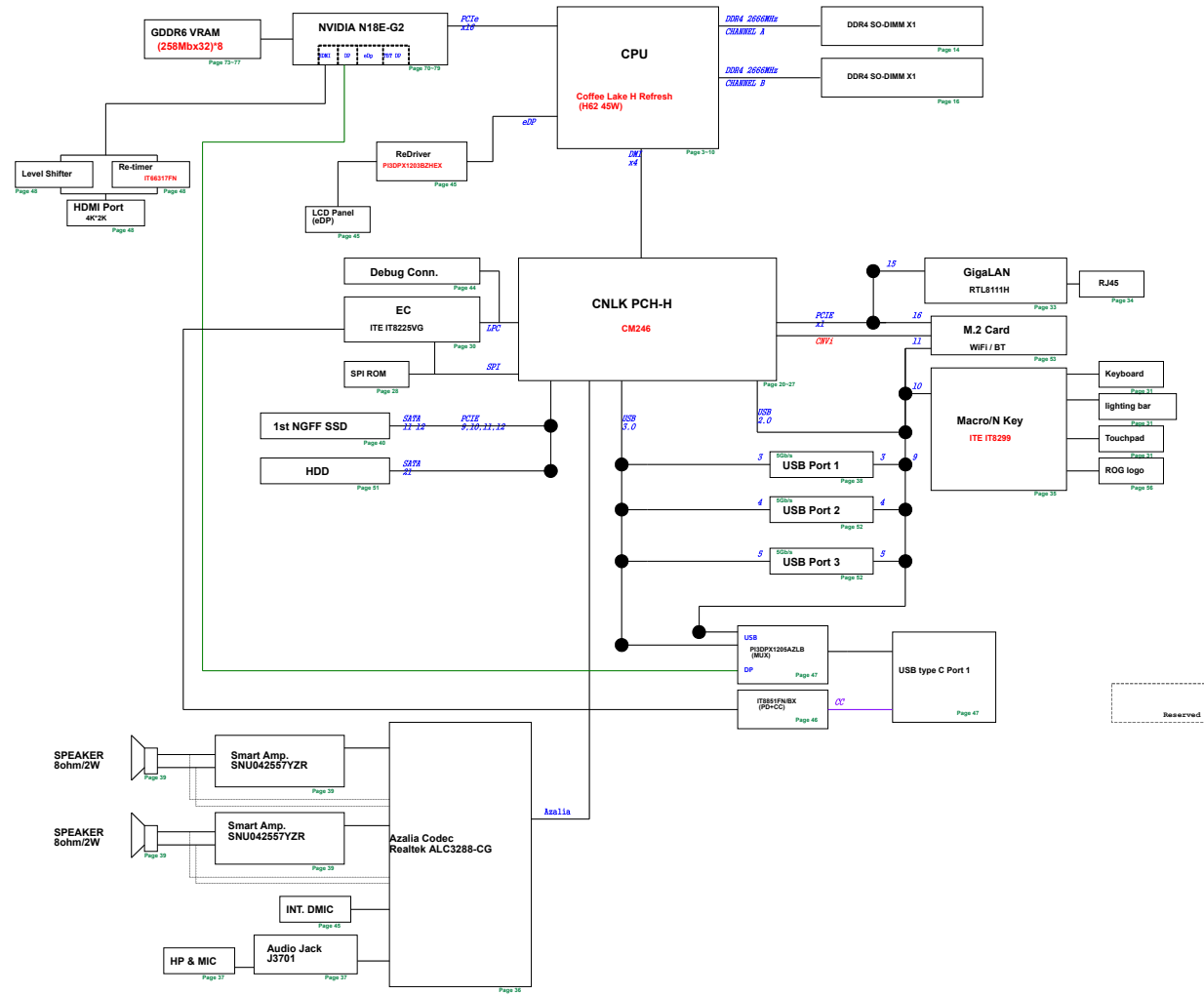


## G531GW Block Diagram

### Coffee Lake H Refresh Platform



Ref	Subject's	Sex	Age	Excluded	MS/POPS	MS/POPS	Phase
REF 01	Subject 1	Male	20	Yes	Yes	Yes	1
REF 02	Subject 2	Female	25	No	Yes	Yes	1
REF 03	Subject 3	Male	30	No	Yes	Yes	1
REF 04	Subject 4	Female	35	No	Yes	Yes	1
REF 05	Subject 5	Male	40	No	Yes	Yes	1
REF 06	Subject 6	Female	45	No	Yes	Yes	1
REF 07	Subject 7	Male	50	No	Yes	Yes	1
REF 08	Subject 8	Female	55	No	Yes	Yes	1
REF 09	Subject 9	Male	60	No	Yes	Yes	1
REF 10	Subject 10	Female	65	No	Yes	Yes	1
REF 11	Subject 11	Male	70	No	Yes	Yes	1
REF 12	Subject 12	Female	75	No	Yes	Yes	1
REF 13	Subject 13	Male	80	No	Yes	Yes	1
REF 14	Subject 14	Female	85	No	Yes	Yes	1
REF 15	Subject 15	Male	90	No	Yes	Yes	1
REF 16	Subject 16	Female	95	No	Yes	Yes	1
REF 17	Subject 17	Male	100	No	Yes	Yes	1
REF 18	Subject 18	Female	105	No	Yes	Yes	1
REF 19	Subject 19	Male	110	No	Yes	Yes	1
REF 20	Subject 20	Female	115	No	Yes	Yes	1
REF 21	Subject 21	Male	120	No	Yes	Yes	1
REF 22	Subject 22	Female	125	No	Yes	Yes	1
REF 23	Subject 23	Male	130	No	Yes	Yes	1
REF 24	Subject 24	Female	135	No	Yes	Yes	1
REF 25	Subject 25	Male	140	No	Yes	Yes	1
REF 26	Subject 26	Female	145	No	Yes	Yes	1
REF 27	Subject 27	Male	150	No	Yes	Yes	1
REF 28	Subject 28	Female	155	No	Yes	Yes	1
REF 29	Subject 29	Male	160	No	Yes	Yes	1
REF 30	Subject 30	Female	165	No	Yes	Yes	1
REF 31	Subject 31	Male	170	No	Yes	Yes	1
REF 32	Subject 32	Female	175	No	Yes	Yes	1
REF 33	Subject 33	Male	180	No	Yes	Yes	1
REF 34	Subject 34	Female	185	No	Yes	Yes	1
REF 35	Subject 35	Male	190	No	Yes	Yes	1
REF 36	Subject 36	Female	195	No	Yes	Yes	1
REF 37	Subject 37	Male	200	No	Yes	Yes	1
REF 38	Subject 38	Female	205	No	Yes	Yes	1
REF 39	Subject 39	Male	210	No	Yes	Yes	1
REF 40	Subject 40	Female	215	No	Yes	Yes	1
REF 41	Subject 41	Male	220	No	Yes	Yes	1
REF 42	Subject 42	Female	225	No	Yes	Yes	1
REF 43	Subject 43	Male	230	No	Yes	Yes	1
REF 44	Subject 44	Female	235	No	Yes	Yes	1
REF 45	Subject 45	Male	240	No	Yes	Yes	1
REF 46	Subject 46	Female	245	No	Yes	Yes	1
REF 47	Subject 47	Male	250	No	Yes	Yes	1
REF 48	Subject 48	Female	255	No	Yes	Yes	1
REF 49	Subject 49	Male	260	No	Yes	Yes	1
REF 50	Subject 50	Female	265	No	Yes	Yes	1
REF 51	Subject 51	Male	270	No	Yes	Yes	1
REF 52	Subject 52	Female	275	No	Yes	Yes	1
REF 53	Subject 53	Male	280	No	Yes	Yes	1
REF 54	Subject 54	Female	285	No	Yes	Yes	1
REF 55	Subject 55	Male	290	No	Yes	Yes	1
REF 56	Subject 56	Female	295	No	Yes	Yes	1
REF 57	Subject 57	Male	300	No	Yes	Yes	1
REF 58	Subject 58	Female	305	No	Yes	Yes	1
REF 59	Subject 59	Male	310	No	Yes	Yes	1
REF 60	Subject 60	Female	315	No	Yes	Yes	1
REF 61	Subject 61	Male	320	No	Yes	Yes	1
REF 62	Subject 62	Female	325	No	Yes	Yes	1
REF 63	Subject 63	Male	330	No	Yes	Yes	1
REF 64	Subject 64	Female	335	No	Yes	Yes	1
REF 65	Subject 65	Male	340	No	Yes	Yes	1
REF 66	Subject 66	Female	345	No	Yes	Yes	1
REF 67	Subject						

Ref	Index/Id	Doc Id	Expected Name	627 P/MS	627 P/MS	Pass
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1997-98	22° 12' N	227	227-100	227-100		

[illegible][illegible]

Year	2000-2001	2001-02	2002-03	2003-04	2004-05	2005-06	2006-07	2007-08	2008-09	2009-10	2010-11	2011-12	2012-13	2013-14	2014-15	2015-16	2016-17	2017-18	2018-19	2019-20	2020-21	2021-22	2022-23	2023-24	2024-25	2025-26	2026-27	2027-28	2028-29	2029-30	2030-31	2031-32	2032-33	2033-34	2034-35	2035-36	2036-37	2037-38	2038-39	2039-40	2040-41	2041-42	2042-43	2043-44	2044-45	2045-46	2046-47	2047-48	2048-49	2049-50	2050-51	2051-52	2052-53	2053-54	2054-55	2055-56	2056-57	2057-58	2058-59	2059-60	2060-61	2061-62	2062-63	2063-64	2064-65	2065-66	2066-67	2067-68	2068-69	2069-70	2070-71	2071-72	2072-73	2073-74	2074-75	2075-76	2076-77	2077-78	2078-79	2079-80	2080-81	2081-82	2082-83	2083-84	2084-85	2085-86	2086-87	2087-88	2088-89	2089-90	2090-91	2091-92	2092-93	2093-94	2094-95	2095-96	2096-97	2097-98	2098-99	2099-00	2100-01	2101-02	2102-03	2103-04	2104-05	2105-06	2106-07	2107-08	2108-09	2109-10	2110-11	2111-12	2112-13	2113-14	2114-15	2115-16	2116-17	2117-18	2118-19	2119-20	2120-21	2121-22	2122-23	2123-24	2124-25	2125-26	2126-27	2127-28	2128-29	2129-30	2130-31	2131-32	2132-33	2133-34	2134-35	2135-36	2136-37	2137-38	2138-39	2139-40	2140-41	2141-42	2142-43	2143-44	2144-45	2145-46	2146-47	2147-48	2148-49	2149-50	2150-51	2151-52	2152-53	2153-54	2154-55	2155-56	2156-57	2157-58	2158-59	2159-60	2160-61	2161-62	2162-63	2163-64	2164-65	2165-66	2166-67	2167-68	2168-69	2169-70	2170-71	2171-72	2172-73	2173-74	2174-75	2175-76	2176-77	2177-78	2178-79	2179-80	2180-81	2181-82	2182-83	2183-84	2184-85	2185-86	2186-87	2187-88	2188-89	2189-90	2190-91	2191-92	2192-93	2193-94	2194-95	2195-96	2196-97	2197-98	2198-99	2199-00	2200-01	2201-02	2202-03	2203-04	2204-05	2205-06	2206-07	2207-08	2208-09	2209-10	2210-11	2211-12	2212-13	2213-14	2214-15	2215-16	2216-17	2217-18	2218-19	2219-20	2220-21	2221-22	2222-23	2223-24	2224-25	2225-26	2226-27	2227-28	2228-29	2229-30	2230-31	2231-32	2232-33	2233-34	2234-35	2235-36	2236-37	2237-38	2238-39	2239-40	2240-41	2241-42	2242-43	2243-44	2244-45	2245-46	2246-47	2247-48	2248-49	2249-50	2250-51	2251-52	2252-53	2253-54	2254-55	2255-56	2256-57	2257-58	2258-59	2259-60	2260-61	2261-62	2262-63	2263-64	2264-65	2265-66	2266-67	2267-68	2268-69	2269-70	2270-71	2271-72	2272-73	2273-74	2274-75	2275-76	2276-77	2277-78	2278-79	2279-80	2280-81	2281-82	2282-83	2283-84	2284-85	2285-86	2286-87	2287-88	2288-89	2289-90	2290-91	2291-92	2292-93	2293-94	2294-95	2295-96	2296-97	2297-98	2298-99	2299-00	2300-01	2301-02	2302-03	2303-04	2304-05	2305-06	2306-07	2307-08	2308-09	2309-10	2310-11	2311-12	2312-13	2313-14	2314-15	2315-16	2316-17	2317-18	2318-19	2319-20	2320-21	2321-22	2322-23	2323-24	2324-25	2325-26	2326-27	2327-28	2328-29	2329-30	2330-31	2331-32	2332-33	2333-34	2334-35	2335-36	2336-37	2337-38	2338-39	2339-40	2340-41	2341-42	2342-43	2343-44	2344-45	2345-46	2346-47	2347-48	2348-49	2349-50	2350-51	2351-52	2352-53	2353-54	2354-55	2355-56	2356-57	2357-58	2358-59	2359-60	2360-61	2361-62	2362-63	2363-64	2364-65	2365-66	2366-67	2367-68	2368-69	2369-70	2370-71	2371-72	2372-73	2373-74	2374-75	2375-76	2376-77	2377-78	2378-79	2379-80	2380-81	2381-82	2382-83	2383-84	2384-85	2385-86	2386-87	2387-88	2388-89	2389-90	2390-91	2391-92	2392-93	2393-94	2394-95	2395-96	2396-97	2397-98	2398-99	2399-00	2400-01	2401-02	2402-03	2403-04	2404-05	2405-06	2406-07	2407-08	2408-09	2409-10	2410-11	2411-12	2412-13	2413-14	2414-15	2415-16	2416-17	2417-18	2418-19	2419-20	2420-21	2421-22	2422-23	2423-24	2424-25	2425-26	2426-27	2427-28	2428-29	2429-30	2430-31	2431-32	2432-33	2433-34	2434-35	2435-36	2436-37	2437-38	2438-39	2439-40	2440-41	2441-42	2442-43	2443-44	2444-45	2445-46	2446-47	2447-48	2448-49	2449-50	2450-51	2451-52	2452-53	2453-54	2454-55	2455-56	2456-57	2457-58	2458-59	2459-60	2460-61	2461-62	2462-63	2463-64	2464-65	2465-66	2466-67	2467-68	2468-69	2469-70	2470-71	2471-72	2472-73	2473-74	2474-75	2475-76	2476-77	2477-78	2478-79	2479-80	2480-81	2481-82	2482-83	2483-84	2484-85	2485-86	2486-87	2487-88	2488-89	2489-90	2490-91	2491-92	2492-93	2493-94	2494-95	2495-96	2496-97	2497-98	2498-99	2499-00	2500-01	2501-02	2502-03	2503-04	2504-05	2505-06	2506-07	2507-08	2508-09	2509-10	2510-11	2511-12	2512-13	2513-14	2514-15	2515-16	2516-17	2517-18	2518-19	2519-20	2520-21	2521-22	2522-23	2523-24	2524-25	2525-26	2526-27	2527-28	2528-29	2529-30	2530-31	2531-32	2532-33	2533-34	2534-35	2535-36	2536-37	2537-38	2538-39	2539-40	2540-41	2541-42	2542-43	2543-44	2544-45	2545-46	2546-47	2547-48	2548-49	2549-50	2550-51	2551-52	2552-53	2553-54	2554-55	2555-56	2556-57	2557-58	2558-59	2559-60	2560-61	2561-62	2562-63	2563-64	2564-65	2565-66	2566-67	2567-68	2568-69	2569-70	2570-71	2571-72	2572-73	2573-74	2574-75	2575-76	2576-77	2577-78	2578-79	2579-80	2580-81	2581-82	2582-83	2583-84	2584-85	2585-86	2586-87	2587-88	2588-89	2589-90	2590-91	2591-92	2592-93	2593-94	2594-95	2595-96	2596-97	2597-98	2598-99	2599-00	2600-01	2601-02	2602-03	2603-04	2604-05	2605-06	2606-07	2607-08	2608-09	2609-10	2610-11	2611-12	2612-13	2613-14	2614-15	2615-16	2616-17	2617-18	2618-19	2619-20	2620-21	2621-22	2622-23	2623-24	2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	Definisi	Das An	Signal Name	EXT(PIN)	Power
0000	0	000	000 000		
0001	1	000	000 001	PO 000 001	1000 W
0002	2	000	000 002 000 000	PO 000 001	1000 W
0003	3-4	000	000 000		
0004	5	000	000 001		
0005	6-15	000	000 000		
0006	16-17	000	00 000 000		
0007	18	000	00 000		

	Defect's ID	Use As	Original Name	ESTIMATE	Period
00000	0.00	0.00	0.00	0.00	0.00
00001	0.01	0.01	0.01	0.01	0.01
00002	0.02	0.02	0.02	0.02	0.02
00003	0.03	0.03	0.03	0.03	0.03
00004	0.04	0.04	0.04	0.04	0.04
00005	0.05	0.05	0.05	0.05	0.05
00006	0.06	0.06	0.06	0.06	0.06
00007	0.07	0.07	0.07	0.07	0.07
00008	0.08	0.08	0.08	0.08	0.08
00009	0.09	0.09	0.09	0.09	0.09
00010	0.10	0.10	0.10	0.10	0.10
00011	0.11	0.11	0.11	0.11	0.11
00012	0.12	0.12	0.12	0.12	0.12
00013	0.13	0.13	0.13	0.13	0.13
00014	0.14	0.14	0.14	0.14	0.14
00015	0.15	0.15	0.15	0.15	0.15
00016	0.16	0.16	0.16	0.16	0.16
00017	0.17	0.17	0.17	0.17	0.17
00018	0.18	0.18	0.18	0.18	0.18
00019	0.19	0.19	0.19	0.19	0.19
00020	0.20	0.20	0.20	0.20	0.20
00021	0.21	0.21	0.21	0.21	0.21
00022	0.22	0.22	0.22	0.22	0.22
00023	0.23	0.23	0.23	0.23	0.23
00024	0.24	0.24	0.24	0.24	0.24
00025	0.25	0.25	0.25	0.25	0.25
00026	0.26	0.26	0.26	0.26	0.26
00027	0.27	0.27	0.27	0.27	0.27
00028	0.28	0.28	0.28	0.28	0.28
00029	0.29	0.29	0.29	0.29	0.29
00030	0.30	0.30	0.30	0.30	0.30
00031	0.31	0.31	0.31	0.31	0.31
00032	0.32	0.32	0.32	0.32	0.32
00033	0.33	0.33	0.33	0.33	0.33
00034	0.34	0.34	0.34	0.34	0.34
00035	0.35	0.35	0.35	0.35	0.35
00036	0.36	0.36	0.36	0.36	0.36
00037	0.37	0.37	0.37	0.37	0.37
00038	0.38	0.38	0.38	0.38	0.38
00039	0.39	0.39	0.39	0.39	0.39
00040	0.40	0.40	0.40	0.40	0.40
00041	0.41	0.41	0.41	0.41	0.41
00042	0.42	0.42	0.42	0.42	0.42
00043	0.43	0.43	0.43	0.43	0.43
00044	0.44	0.44	0.44	0.44	0.44
00045	0.45	0.45	0.45	0.45	0.45
00046	0.46	0.46	0.46	0.46	0.46
00047	0.47	0.47	0.47	0.47	0.47
00048	0.48	0.48	0.48	0.48	0.48
00049	0.49	0.49	0.49	0.49	0.49
00050	0.50	0.50	0.50	0.50	0.50
00051	0.51	0.51	0.51	0.51	0.51
00052	0.52	0.52	0.52	0.52	0.52
00053	0.53	0.53	0.53	0.53	0.53
00054	0.54	0.54	0.54	0.54	0.54
00055	0.55	0.55	0.55	0.55	0.55
00056	0.56	0.56	0.56	0.56	0.56
00057	0.57	0.57	0.57	0.57	0.57
00058	0.58	0.58	0.58	0.58	0.58
00059	0.59	0.59	0.59	0.59	0.59
00060	0.60	0.60	0.60	0.60	0.60
00061	0.61	0.61	0.61	0.61	0.61
00062	0.62	0.62	0.62	0.62	0.62
00063	0.63	0.63	0.63	0.63	0.63
00064	0.64	0.64	0.64	0.64	0.64
00065	0.65	0.65	0.65	0.65	0.65
00066	0.66	0.66	0.66	0.66	0.66
00067	0.67	0.67	0.67	0.67	0.67
00068	0.68	0.68	0.68	0.68	0.68
00069	0.69	0.69	0.69	0.69	0.69
00070	0.70	0.70	0.70	0.70	0.70
00071	0.71	0.71	0.71	0.71	0.71
00072	0.72	0.72	0.72	0.72	0.72
00073	0.73	0.73	0.73	0.73	0.73
00074	0.74	0.74	0.74	0.74	0.74
00075	0.75	0.75	0.75	0.75	0.75
00076	0.76	0.76	0.76	0.76	0.76
00077	0.77	0.77	0.77	0.77	0.77
00078	0.78	0.78	0.78	0.78	0.78
00079	0.79	0.79	0.79	0.79	0.79
00080	0.80	0.80	0.80	0.80	0.80
00081	0.81	0.81	0.81	0.81	0.81
00082	0.82	0.82	0.82	0.82	0.82
00083	0.83	0.83	0.83	0.83	0.83
00084	0.84	0.84	0.84	0.84	0.84
00085	0.85	0.85	0.85	0.85	0.85
00086	0.86	0.86	0.86	0.86	0.86
00087	0.87	0.87	0.87	0.87	0.87
00088	0.88	0.88	0.88	0.88	0.88
00089	0.89	0.89	0.89	0.89	0.89
00090	0.90	0.90	0.90	0.90	0.90
00091	0.91	0.91	0.91	0.91	0.91
00092	0.92	0.92	0.92	0.92	0.92
00093	0.93	0.93	0.93	0.93	0.93
00094	0.94	0.94	0.94	0.94	0.94
00095	0.95	0.95	0.95	0.95	0.95
00096	0.96	0.96	0.96	0.96	0.96
00097	0.97	0.97	0.97	0.97	0.97
00098	0.98	0.98	0.98	0.98	0.98
00099	0.99	0.99	0.99	0.99	0.99
00100	1.00	1.00	1.00	1.00	1.00

	Subject	Use As	Original Name	EXPENSE	Notes
0001	0	001	00 00000000 00 00		
0002	0	001	00 00000000 00 00		
0003	0	001	00 00000000 00 00		
0004	0	001	00 00000000 00 00		
0005	0	001	00 00000000 00 00		
0006	0	001	00 00000000 00 00		
0007	0	001	00 00000000 00 00		
0008	0	001	00 00000000 00 00		
0009	0	001	00 00000000 00 00		
0010	0	001	00 00000000 00 00		
0011	0	001	00 00000000 00 00		
0012	0	001	00 00000000 00 00		
0013	0	001	00 00000000 00 00		
0014	0	001	00 00000000 00 00		
0015	0	001	00 00000000 00 00		
0016	0	001	00 00000000 00 00		
0017	0	001	00 00000000 00 00		
0018	0	001	00 00000000 00 00		
0019	0	001	00 00000000 00 00		
0020	0	001	00 00000000 00 00		
0021	0	001	00 00000000 00 00		
0022	0	001	00 00000000 00 00		
0023	0	001	00 00000000 00 00		
0024	0	001	00 00000000 00 00		
0025	0	001	00 00000000 00 00		
0026	0	001	00 00000000 00 00		
0027	0	001	00 00000000 00 00		
0028	0	001	00 00000000 00 00		
0029	0	001	00 00000000 00 00		
0030	0	001	00 00000000 00 00		
0031	0	001	00 00000000 00 00		
0032	0	001	00 00000000 00 00		
0033	0	001	00 00000000 00 00		
0034	0	001	00 00000000 00 00		
0035	0	001	00 00000000 00 00		
0036	0	001	00 00000000 00 00		
0037	0	001	00 00000000 00 00		
0038	0	001	00 00000000 00 00		
0039	0	001	00 00000000 00 00		
0040	0	001	00 00000000 00 00		
0041	0	001	00 00000000 00 00		
0042	0	001	00 00000000 00 00		
0043	0	001	00 00000000 00 00		
0044	0	001	00 00000000 00 00		
0045	0	001	00 00000000 00 00		
0046	0	001	00 00000000 00 00		
0047	0	001	00 00000000 00 00		
0048	0	001	00 00000000 00 00		
0049	0	001	00 00000000 00 00		
0050	0	001	00 00000000 00 00		
0051	0	001	00 00000000 00 00		
0052	0	001	00 00000000 00 00		
0053	0	001	00 00000000 00 00		
0054	0	001	00 00000000 00 00		
0055	0	001	00 00000000 00 00		
0056	0	001	00 00000000 00 00		
0057	0	001	00 00000000 00 00		
0058	0	001	00 00000000 00 00		
0059	0	001	00 00000000 00 00		
0060	0	001	00 00000000 00 00		
0061	0	001	00 00000000 00 00		
0062	0	001	00 00000000 00 00		
0063	0	001	00 00000000 00 00		
0064	0	001	00 00000000 00 00		
0065	0	001	00 00000000 00 00		
0066	0	001	00 00000000 00 00		
0067	0	001	00 00000000 00 00		
0068	0	001	00 00000000 00 00		
0069	0	001	00 00000000 00 00		
0070	0	001	00 00000000 00 00		
0071	0	001	00 00000000 00 00		
0072	0	001	00 00000000 00 00		
0073	0	001	00 00000000 00 00		
0074	0	001	00 00000000 00 00		
0075	0	001	00 00000000 00 00		
0076	0	001	00 00000000 00 00		
0077	0	001	00 00000000 00 00		
0078	0	001	00 00000000 00 00		
0079	0	001	00 00000000 00 00		
0080	0	001	00 00000000 00 00		
0081	0	001	00 00000000 00 00		
0082	0	001	00 00000000 00 00		
0083	0	001	00 00000000 00 00		
0084	0	001	00 00000000 00 00		
0085	0	001	00 00000000 00 00		
0086	0	001	00 00000000 00 00		
0087	0	001	00 00000000 00 00		
0088	0	001	00 00000000 00 00		
0089	0	001	00 00000000 00 00		
0090	0	001	00 00000000 00 00		
0091	0	001	00 00000000 00 00		
0092	0	001	00 00000000 00 00		
0093	0	001	00 00000000 00 00		
0094	0	001	00 00000000 00 00		
0095	0	001	00 00000000 00 00		
0096	0	001	00 00000000 00 00		
0097	0	001	00 00000000 00 00		
0098	0	001	00 00000000 00 00		
0099	0	001	00 00000000 00 00		
0100	0	001	00 00000000 00 00		

	Subtask	Use As	Original Name	RePathName	Power
0000	0	0000	0000 0000	00 000000 00	0000 00
0001	0	0001	0000 0000	00 000000 00	0000 00
0002	001	0002	00 0000 0000	00 000000 00	0000 00
0003	001	0003	00 0000 0000	00 000000 00	0000 00
0004	001	0004	00 0000 0000	00 000000 00	0000 00
0005	001	0005	00 0000 0000	00 000000 00	0000 00
0006	001	0006	00 0000 0000	00 000000 00	0000 00
0007	001	0007	00 0000 0000	00 000000 00	0000 00
0008	001	0008	00 0000 0000	00 000000 00	0000 00
0009	001	0009	00 0000 0000	00 000000 00	0000 00
0010	001	0010	00 0000 0000	00 000000 00	0000 00
0011	001	0011	00 0000 0000	00 000000 00	0000 00
0012	001	0012	00 0000 0000	00 000000 00	0000 00
0013	001	0013	00 0000 0000	00 000000 00	0000 00
0014	001	0014	00 0000 0000	00 000000 00	0000 00
0015	001	0015	00 0000 0000	00 000000 00	0000 00
0016	001	0016	00 0000 0000	00 000000 00	0000 00
0017	001	0017	00 0000 0000	00 000000 00	0000 00
0018	001	0018	00 0000 0000	00 000000 00	0000 00
0019	001	0019	00 0000 0000	00 000000 00	0000 00
0020	001	0020	00 0000 0000	00 000000 00	0000 00
0021	001	0021	00 0000 0000	00 000000 00	0000 00
0022	001	0022	00 0000 0000	00 000000 00	0000 00
0023	001	0023	00 0000 0000	00 000000 00	0000 00
0024	001	0024	00 0000 0000	00 000000 00	0000 00
0025	001	0025	00 0000 0000	00 000000 00	0000 00
0026	001	0026	00 0000 0000	00 000000 00	0000 00
0027	001	0027	00 0000 0000	00 000000 00	0000 00
0028	001	0028	00 0000 0000	00 000000 00	0000 00
0029	001	0029	00 0000 0000	00 000000 00	0000 00
0030	001	0030	00 0000 0000	00 000000 00	0000 00
0031	001	0031	00 0000 0000	00 000000 00	0000 00
0032	001	0032	00 0000 0000	00 000000 00	0000 00
0033	001	0033	00 0000 0000	00 000000 00	0000 00
0034	001	0034	00 0000 0000	00 000000 00	0000 00
0035	001	0035	00 0000 0000	00 000000 00	0000 00
0036	001	0036	00 0000 0000	00 000000 00	0000 00
0037	001	0037	00 0000 0000	00 000000 00	0000 00
0038	001	0038	00 0000 0000	00 000000 00	0000 00
0039	001	0039	00 0000 0000	00 000000 00	0000 00
0040	001	0040	00 0000 0000	00 000000 00	0000 00
0041	001	0041	00 0000 0000	00 000000 00	0000 00
0042	001	0042	00 0000 0000	00 000000 00	0000 00
0043	001	0043	00 0000 0000	00 000000 00	0000 00
0044	001	0044	00 0000 0000	00 000000 00	0000 00
0045	001	0045	00 0000 0000	00 000000 00	0000 00
0046	001	0046	00 0000 0000	00 000000 00	0000 00
0047	001	0047	00 0000 0000	00 000000 00	0000 00
0048	001	0048	00 0000 0000	00 000000 00	0000 00
0049	001	0049	00 0000 0000	00 000000 00	0000 00
0050	001	0050	00 0000 0000	00 000000 00	0000 00
0051	001	0051	00 0000 0000	00 000000 00	00

[illegible]

Set	DefSet	Set As	Original Name	EXTNAME	Power
0000	Default 0	SP0	SP0 (SP0) - SP0000	SP0	0.0000
0001	0	SP1	SP1 (SP1) - SP0001	SP1	0.0001
0002	0	SP2	SP2 (SP2) - SP0002	SP2	0.0002
0003	0	SP3	SP3 (SP3) - SP0003	SP3	0.0003
0004	0	SP4	SP4 (SP4) - SP0004	SP4	0.0004
0005	0	SP5	SP5 (SP5) - SP0005	SP5	0.0005
0006	0	SP6	SP6 (SP6) - SP0006	SP6	0.0006
0007	0	SP7	SP7 (SP7) - SP0007	SP7	0.0007
0008	0	SP8	SP8 (SP8) - SP0008	SP8	0.0008
0009	0	SP9	SP9 (SP9) - SP0009	SP9	0.0009
0010	0	SP10	SP10 (SP10) - SP0010	SP10	0.0010
0011	0	SP11	SP11 (SP11) - SP0011	SP11	0.0011
0012	0	SP12	SP12 (SP12) - SP0012	SP12	0.0012
0013	0	SP13	SP13 (SP13) - SP0013	SP13	0.0013
0014	0	SP14	SP14 (SP14) - SP0014	SP14	0.0014
0015	0	SP15	SP15 (SP15) - SP0015	SP15	0.0015
0016	0	SP16	SP16 (SP16) - SP0016	SP16	0.0016
0017	0	SP17	SP17 (SP17) - SP0017	SP17	0.0017
0018	0	SP18	SP18 (SP18) - SP0018	SP18	0.0018
0019	0	SP19	SP19 (SP19) - SP0019	SP19	0.0019
0020	0	SP20	SP20 (SP20) - SP0020	SP20	0.0020
0021	0	SP21	SP21 (SP21) - SP0021	SP21	0.0021
0022	0	SP22	SP22 (SP22) - SP0022	SP22	0.0022
0023	0	SP23	SP23 (SP23) - SP0023	SP23	0.0023
0024	0	SP24	SP24 (SP24) - SP0024	SP24	0.0024
0025	0	SP25	SP25 (SP25) - SP0025	SP25	0.0025
0026	0	SP26	SP26 (SP26) - SP0026	SP26	0.0026
0027	0	SP27	SP27 (SP27) - SP0027	SP27	0.0027
0028	0	SP28	SP28 (SP28) - SP0028	SP28	0.0028
0029	0	SP29	SP29 (SP29) - SP0029	SP29	0.0029
0030	0	SP30	SP30 (SP30) - SP0030	SP30	0.0030
0031	0	SP31	SP31 (SP31) - SP0031	SP31	0.0031
0032	0	SP32	SP32 (SP32) - SP0032	SP32	0.0032
0033	0	SP33	SP33 (SP33) - SP0033	SP33	0.0033
0034	0	SP34	SP34 (SP34) - SP0034	SP34	0.0034
0035	0	SP35	SP35 (SP35) - SP0035	SP35	0.0035
0036	0	SP36	SP36 (SP36) - SP0036	SP36	0.0036
0037	0	SP37	SP37 (SP37) - SP0037	SP37	0.0037
0038	0	SP38	SP38 (SP38) - SP0038	SP38	0.0038
0039	0	SP39	SP39 (SP39) - SP0039	SP39	0.0039
0040	0	SP40	SP40 (SP40) - SP0040	SP40	0.0040
0041	0	SP41	SP41 (SP41) - SP0041	SP41	0.0041
0042	0	SP42	SP42 (SP42) - SP0042	SP42	0.0042
0043	0	SP43	SP43 (SP43) - SP0043	SP43	0.0043
0044	0	SP44	SP44 (SP44) - SP0044	SP44	0.0044
0045	0	SP45	SP45 (SP45) - SP0045	SP45	0.0045
0046	0	SP46	SP46 (SP46) - SP0046	SP46	0.0046
0047	0	SP47	SP47 (SP47) - SP0047	SP47	0.0047
0048	0	SP48	SP48 (SP48) - SP0048	SP48	0.0048
0049	0	SP49	SP49 (SP49) - SP0049	SP49	0.0049
0050	0	SP50	SP50 (SP50) - SP0050	SP50	0.0050
0051	0	SP51	SP51 (SP51) - SP0051	SP51	0.0051
0052	0	SP52	SP52 (SP52) - SP0052	SP52	0.0052
0053	0	SP53	SP53 (SP53) - SP0053	SP53	0.0053
0054	0	SP54	SP54 (SP54) - SP0054	SP54	0.0054
0055	0	SP55	SP55 (SP55) - SP0055	SP55	0.0055
0056	0	SP56	SP56 (SP56) - SP0056	SP56	0.0056
0057	0	SP57	SP57 (SP57) - SP0057	SP57	0.0057
0058	0	SP58	SP58 (SP58) - SP0058	SP58	0.0058
0059	0	SP59	SP59 (SP59) - SP0059	SP59	0.0059
0060	0	SP60	SP60 (SP60) - SP0060	SP60	0.0060

Index	SSIC#	SSIC#	SSIC#	SSIC#	SSIC#
SSIC# PCN-31 Z170 H580					
1	USBS#1 (YOT0)				1
2	USBS#2	SSIC#1			2
3	USBS#3	SSIC#2			3
4	USBS#4				4
5	USBS#5				5
6	USBS#6				6
7	USBS#7	PCIE#1	x/2		7
8	USBS#8	PCIE#2			8
9	USBS#9	PCIE#3			9
10	USBS#10	PCIE#4	6/8	x/2	10

12	PCB #9		x/2	NA	12	PCB #6		
13	PCB #7		x/2		13	PCB #8		
14	PCB #9		x/2		14	PCB #9		
15	PCB #9	SATA 50	Chd	x/2	used RST	15	PCB #9	SA
16	PCB #10	SATA #1		x/2	PCB Storage	16	PCB #10	SA
17	PCB #11			x/2	Device #1	17	PCB #11	
18	PCB #12		Chd	x/2		18	PCB #12	
19	PCB #13	SATA #07	Chd	x/2		19	PCB #13	SA
20	PCB #14	SATA #11		x/2	used RST	20	PCB #14	SA
21	PCB #15	SATA #20		x/2	PCB Storage	21	PCB #15	SA
22	PCB #16	SATA #15		x/2	Device #2	22	PCB #16	
23	PCB #17	SATA #14		x/2		23	SATA #15	
24	PCB #18	SATA #5		x/2	used RST	24	SATA #16	
25	PCB #19			x/2	PCB Storage	25	PCB #19	
26	PCB #20	SATA #2		x/2	Device #5	26	PCB #20	

### N501VW Setting

SW, BUS ADDRESS :		
PCN Manager		
300 Bus Address		
00000000 (000)	SW	SW Bus Address
00000001 (001)		
00000002 (002)		
00000003 (003)		
00000004 (004)		
00000005 (005)		
00000006 (006)		
00000007 (007)		
00000008 (008)		
00000009 (009)		
0000000A (010)		
0000000B (011)		
0000000C (012)		
0000000D (013)		
0000000E (014)		
0000000F (015)		
00000010 (016)		
00000011 (017)		
00000012 (018)		
00000013 (019)		
00000014 (020)		
00000015 (021)		
00000016 (022)		
00000017 (023)		
00000018 (024)		
00000019 (025)		
0000001A (026)		
0000001B (027)		
0000001C (028)		
0000001D (029)		
0000001E (030)		
0000001F (031)		
00000020 (032)		
00000021 (033)		
00000022 (034)		
00000023 (035)		
00000024 (036)		
00000025 (037)		
00000026 (038)		
00000027 (039)		
00000028 (040)		
00000029 (041)		
0000002A (042)		
0000002B (043)		
0000002C (044)		
0000002D (045)		
0000002E (046)		
0000002F (047)		
00000030 (048)		
00000031 (049)		
00000032 (050)		
00000033 (051)		
00000034 (052)		
00000035 (053)		
00000036 (054)		
00000037 (055)		
00000038 (056)		
00000039 (057)		
0000003A (058)		
0000003B (059)		
0000003C (060)		
0000003D (061)		
0000003E (062)		
0000003F (063)		
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00000042 (066)		
00000043 (067)		
00000044 (068)		
00000045 (069)		
00000046 (070)		
00000047 (071)		
00000048 (072)		
00000049 (073)		
0000004A (074)		
0000004B (075)		
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0000004D (077)		
0000004E (078)		
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00000051 (081)		
00000052 (082)		
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00000057 (087)		
00000058 (088)		
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0000005B (091)		
0000005C (092)		
0000005D (093)		
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00000069 (105)		
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000000A4 (164)		
000000A5 (165)		
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000000A7 (167)		
000000A8 (168)		
000000A9 (169)		
000000AA (170)		
000000AB (171)		
000000AC (172)		
000000AD (173)		
000000AE (174)		
000000AF (175)		
000000B0 (176)		
000000B1 (177)		
000000B2 (178)		
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000000B6 (182)		
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000000B8 (184)		
000000B9 (185)		
000000BA (186)		
000000BB (187)		
000000BC (188)		
000000BD (189)		
000000BE (190)		
000000BF (191)		
000000C0 (192)		
000000C1 (193)		
000000C2 (194)		
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000000C6 (198)		
000000C7 (199)		
000000C8 (200)		
000000C9 (201)		
000000CA (202)		
000000CB (203)		
000000CC (204)		
000000CD (205)		
000000CE (206)		
000000CF (207)		
000000D0 (208)		
000000D1 (209)		
000000D2 (210)		
000000D3 (211)		
000000D4 (212)		
000000D5 (213)		
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000000D8 (216)		
000000D9 (217)		
000000DA (218)		
000000DB (219)		
000000DC (220)		
000000DD (221)		
000000DE (222)		
000000DF (223)		
000000E0 (224)		
000000E1 (225)		
000000E2 (226)		
000000E3 (227)		
000000E4 (228)		
000000E5 (229)		
000000E6 (230)		
000000E7 (231)		
000000E8 (232)		
000000E9 (233)		
000000EA (234)		
000000EB (235)		
000000EC (236)		
000000ED (237)		
000000EE (238)		
000000EF (239)		
000000F0 (240)		
000000F1 (241)		
000000F2 (242)		
000000F3 (243)		
000000F4 (244)		
000000F5 (245)		
000000F6 (246)		
000000F7 (247)		
000000F8 (248)		
000000F9 (249)		
000000FA (250)		
000000FB (251)		
000000FC (252)		
000000FD (253)		
000000FE (254)		
000000FF (255)		

Device Identification		
PCN Hardware Revision		
SW	Manufacturer ID	Manufacturer

### DECLARATIONS & USE Function Define

Age	First experience	Partner	Age	First experience	Partner
16	First time (2002)	John	2003		
17	First time (2003)	John	2004		
18	First time (2003)	John	2005		
19	First time (2003)	John	2006		
20	First time (2003)	John	2007		
21	First time (2003)	John	2008		
22	First time (2003)	John	2009		
23	First time (2003)	John	2010		
24	First time (2003)	John	2011		
25	First time (2003)	John	2012		
26	First time (2003)	John	2013		
27	First time (2003)	John	2014		
28	First time (2003)	John	2015		
29	First time (2003)	John	2016		
30	First time (2003)	John	2017		
31	First time (2003)	John	2018		
32	First time (2003)	John	2019		
33	First time (2003)	John	2020		
34	First time (2003)	John	2021		
35	First time (2003)	John	2022		
36	First time (2003)	John	2023		
37	First time (2003)	John	2024		
38	First time (2003)	John	2025		
39	First time (2003)	John	2026		
40	First time (2003)	John	2027		
41	First time (2003)	John	2028		
42	First time (2003)	John	2029		
43	First time (2003)	John	2030		
44	First time (2003)	John	2031		
45	First time (2003)	John	2032		
46	First time (2003)	John	2033		
47	First time (2003)	John	2034		
48	First time (2003)	John	2035		
49	First time (2003)	John	2036		
50	First time (2003)	John	2037		
51	First time (2003)	John	2038		
52	First time (2003)	John	2039		
53	First time (2003)	John	2040		
54	First time (2003)	John	2041		
55	First time (2003)	John	2042		
56	First time (2003)	John	2043		
57	First time (2003)	John	2044		
58	First time (2003)	John	2045		
59	First time (2003)	John	2046		
60	First time (2003)	John	2047		
61	First time (2003)	John	2048		
62	First time (2003)	John	2049		
63	First time (2003)	John	2050		
64	First time (2003)	John	2051		
65	First time (2003)	John	2052		
66	First time (2003)	John	2053		
67	First time (2003)	John	2054		
68	First time (2003)	John	2055		
69	First time (2003)	John	2056		
70	First time (2003)	John	2057		
71	First time (2003)	John	2058		
72	First time (2003)	John	2059		
73	First time (2003)	John	2060		
74	First time (2003)	John	2061		
75	First time (2003)	John	2062		
76	First time (2003)	John	2063		
77	First time (2003)	John	2064		
78	First time (2003)	John	2065		
79	First time (2003)	John	2066		
80	First time (2003)	John	2067		
81	First time (2003)	John	2068		
82	First time (2003)	John	2069		
83	First time (2003)	John	2070		
84	First time (2003)	John	2071		
85	First time (2003)	John	2072		
86	First time (2003)	John	2073		
87	First time (2003)	John	2074		
88	First time (2003)	John	2075		
89	First time (2003)	John	2076		
90	First time (2003)	John	2077		
91	First time (2003)	John	2078		
92	First time (2003)	John	2079		
93	First time (2003)	John	2080		
94	First time (2003)	John	2081		
95	First time (2003)	John	2082		
96	First time (2003)	John	2083		
97	First time (2003)	John	2084		
98	First time (2003)	John	2085		
99	First time (2003)	John	2086		

PCB: PCH #1 Z170 H510					
1	USER #1 (JOT)				
2	USER #2			SSIC #1	
3	USER #3			SSIC #2	
4	USER #4				
5	USER #5				
6	USER #6				
7	USER #7	PCIE #1			
8	USER #8	PCIE #2	x,2		
9	USER #9	PCIE #3		x,4	NA
10	USER #10	PCIE #4			
11	PCIE #5		QoS		
12	PCIE #6				
13	PCIE #7			x,4	NA
14	PCIE #8				
15	PCIE #9	SATA #6	QoS		
16	PCIE #10	SATA #1		x,4	
17	PCIE #11				VM D1T1 PCIE Staging Device #1
18	PCIE #12	QoS			
19	PCIE #13	SATA #7	QoS		VM D1T1
20	PCIE #14	SATA #1'			
21	PCIE #15	SATA #5	x,2		PCIE Staging Device #2
22	PCIE #16	SATA #3			
23	PCIE #17	SATA #4			VM D1T1
24	PCIE #18	SATA #5		x,4	PCIE Staging Device #3
25	PCIE #19				
26	PCIE #20	SATA #7'			

SBC, PCE #1: H170: P100				
1	1:UNDI #1 (E10)			
2	2:UNDI #2	SSIC #1		
3	3:UNDI #3	SSIC #2		
4	4:UNDI #4			
5	5:UNDI #5			
6	6:UNDI #6			
7	7:UNDI #7			
8	8:UNDI #8			
9	9:MPCE #1		x/2	NA
10	10:MPCE #1	CSIC		
11	11:MPCE #5	CSIC	x/2	
12	12:MPCE #6			
13	13:MPCE #7		x/2	
14	14:MPCE #8			
15	15:MPCE #9	SATA #0	CSIC	
16	16:MPCE #10	SATA #1		
17	17:MPCE #11			
18	18:MPCE #12	CSIC	x/2	
19	19:MPCE #13	SATA #0	CSIC	
20	20:MPCE #14	SATA #1		
21	21:MPCE #15	SATA #2	x/2	
22	22:MPCE #16	SATA #3		
23	23:BA1X#A			
24	24:BA1X#B			
25	25:MPCE #17		NA	NA
26	26:MPCE #20			

SOCI. PSCH. #1 PART 10: VIDEO									
1	VIDEO #1 (OTG)								
2	VIDEO #2								
3	VIDEO #3								
4	VIDEO #4								
5	VIDEO #5								
6	VIDEO #6								
7	VIDEO #7								
8	VIDEO #8								
9	VIDEO #9								
10	VIDEO #10								
11	VIDEO #11								
12	VIDEO #12								
13	VIDEO #13								
14	VIDEO #14								
15	VIDEO #15								
16	VIDEO #16								
17	VIDEO #17								
18	VIDEO #18								
19	VIDEO #19								
20	VIDEO #20								
21	VIDEO #21								
22	VIDEO #22								
23	VIDEO #23								
24	VIDEO #24								
25	VIDEO #25								
26	VIDEO #26								



PCIEG



CFD2=0 -> Reversed  
CFD3=0 -> PCIEG 2x8



PCIEG_T0P_0	CFD2=0	1	0.225F/3V	PCIEG_R0P_0	CFD2=0	1	0.225F/3V
PCIEG_T0P_1	CFD2=0	2	0.225F/3V	PCIEG_R0P_1	CFD2=0	2	0.225F/3V
PCIEG_T0P_2	CFD2=0	3	0.225F/3V	PCIEG_R0P_2	CFD2=0	3	0.225F/3V
PCIEG_T0P_3	CFD2=0	4	0.225F/3V	PCIEG_R0P_3	CFD2=0	4	0.225F/3V
PCIEG_T0P_4	CFD2=0	5	0.225F/3V	PCIEG_R0P_4	CFD2=0	5	0.225F/3V
PCIEG_T0P_5	CFD2=0	6	0.225F/3V	PCIEG_R0P_5	CFD2=0	6	0.225F/3V
PCIEG_T0P_6	CFD2=0	7	0.225F/3V	PCIEG_R0P_6	CFD2=0	7	0.225F/3V
PCIEG_T0P_7	CFD2=0	8	0.225F/3V	PCIEG_R0P_7	CFD2=0	8	0.225F/3V
PCIEG_T0P_8	CFD2=0	9	0.225F/3V	PCIEG_R0P_8	CFD2=0	9	0.225F/3V
PCIEG_T0P_9	CFD2=0	10	0.225F/3V	PCIEG_R0P_9	CFD2=0	10	0.225F/3V
PCIEG_T0P_10	CFD2=0	11	0.225F/3V	PCIEG_R0P_10	CFD2=0	11	0.225F/3V
PCIEG_T0P_11	CFD2=0	12	0.225F/3V	PCIEG_R0P_11	CFD2=0	12	0.225F/3V
PCIEG_T0P_12	CFD2=0	13	0.225F/3V	PCIEG_R0P_12	CFD2=0	13	0.225F/3V
PCIEG_T0P_13	CFD2=0	14	0.225F/3V	PCIEG_R0P_13	CFD2=0	14	0.225F/3V
PCIEG_T0P_14	CFD2=0	15	0.225F/3V	PCIEG_R0P_14	CFD2=0	15	0.225F/3V
PCIEG_T0P_15	CFD2=0	16	0.225F/3V	PCIEG_R0P_15	CFD2=0	16	0.225F/3V

Display

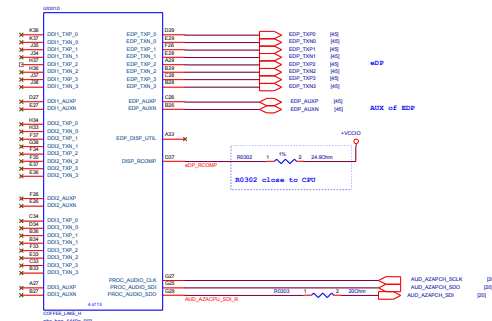


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes													
				0	1	2	3	4	5	6	7	8	9	10	11	12	13
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13
x8	Off	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2

**Notes:**

- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
  - Connect lane 0 of 1st device to lane 0.
  - Connect lane 0 of 2nd device to lane 8.
  - Connect lane 0 of 3rd device to lane 12.For example:
  - a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
  - b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
  - c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane12.

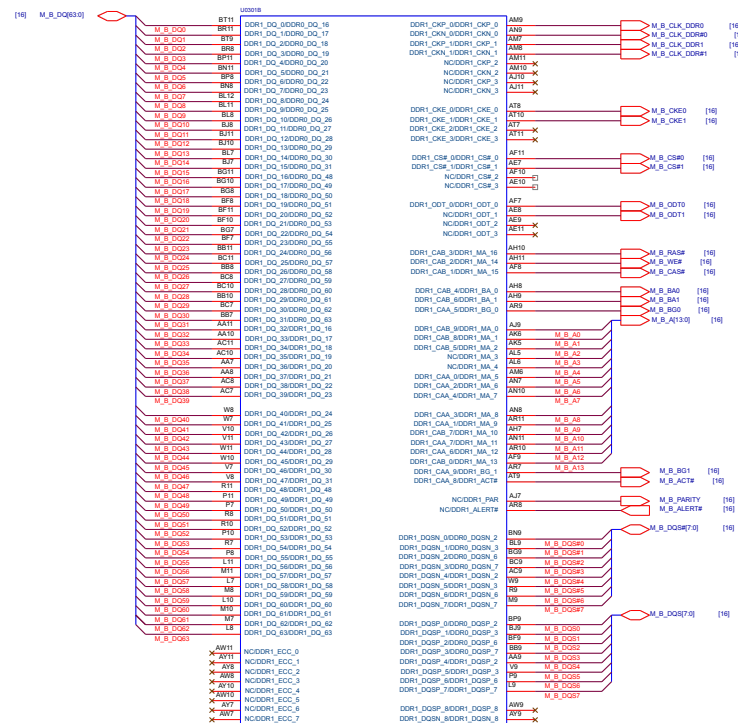
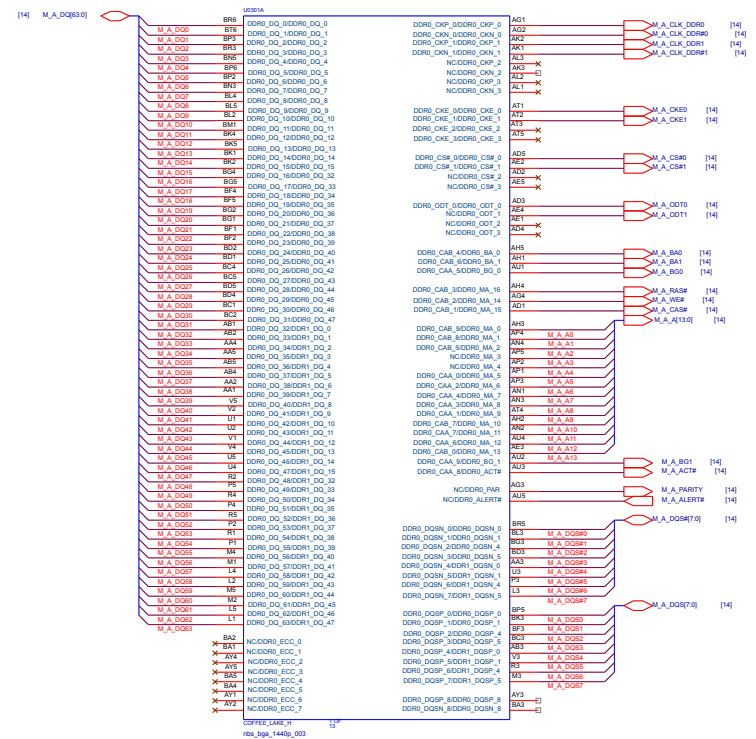
Refer to CFI-8, ROG P.363 (Doc.571391)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA\_SDIN[1:0], DISPA\_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

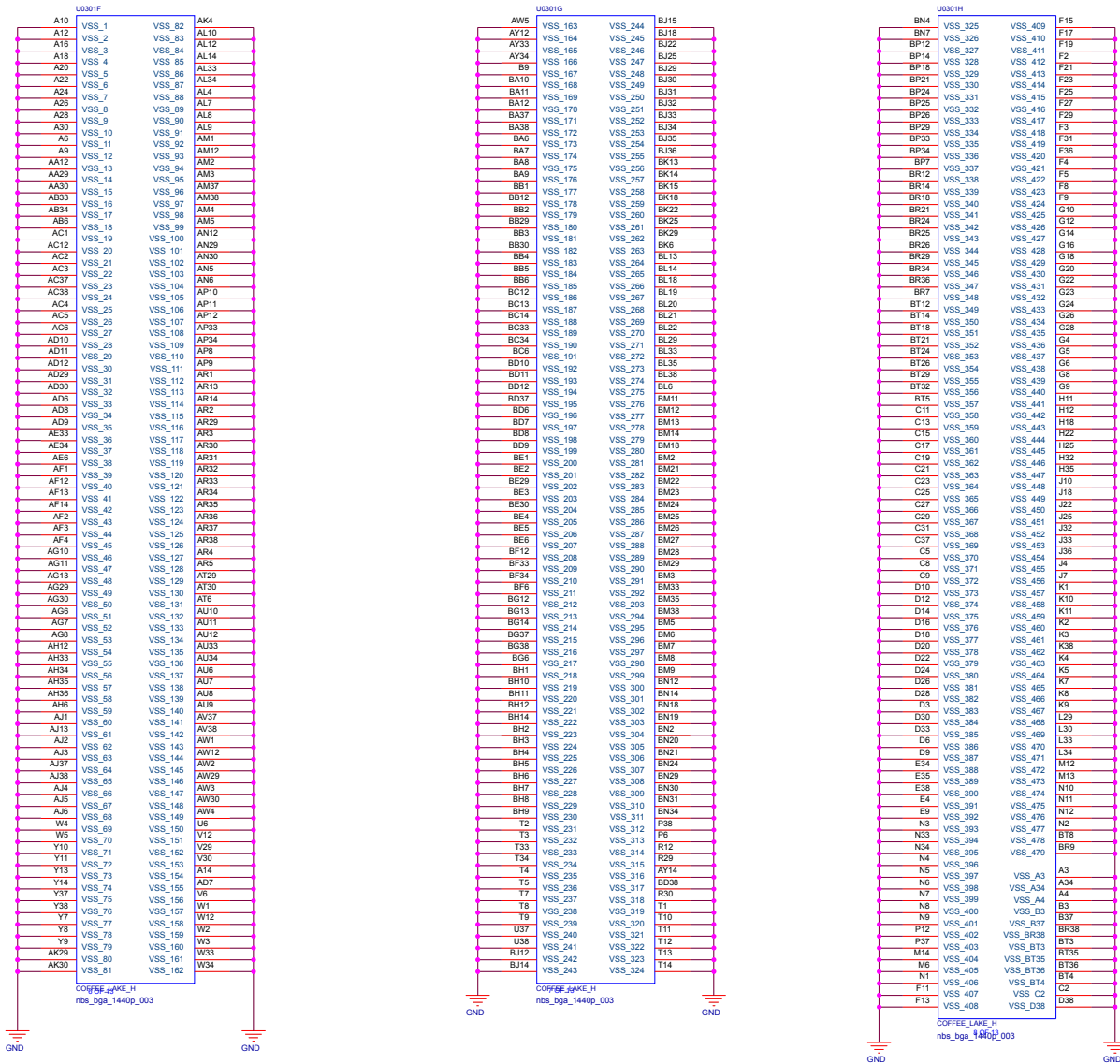
When the Intel® Display Audio interface is not implemented, PROC\_AUDIO\_CLK and PROC\_AUDIO\_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ). PROC\_AUDIO\_SDO can be left unconnected.

ASUS		Project Name	Rev
G711GW			01.1
Title : CPU DRAM/Storage/BIOS			
Doc	Dept: ASUS/COMPUTER	Engineer: Gaming RD	
Date: Tuesday, March 19, 2019	Drawn	3	of 100



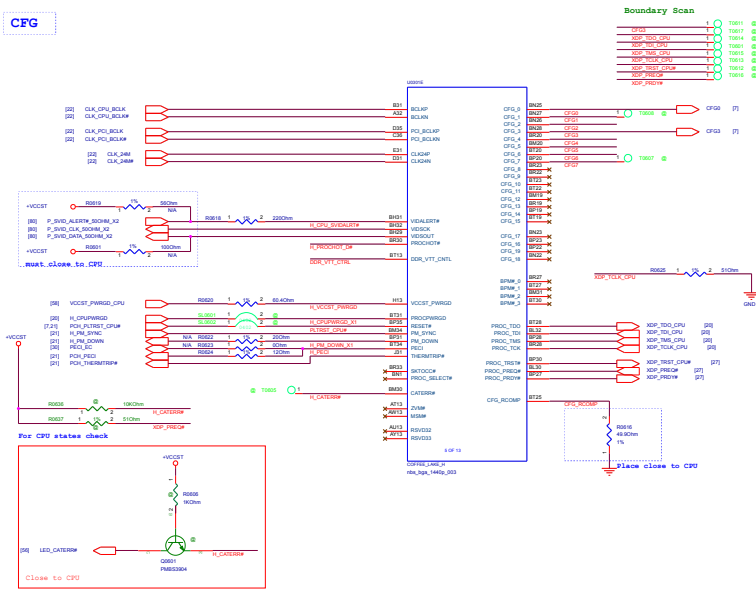


Main Board



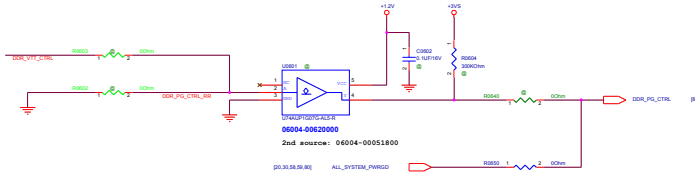
Project Name		Rev
ASUS G711GW		1.0
Title : CPU_CFG,RSDV,GND		
Size	Dept.: ASUSTek COMPUTER	Engineer: Gaming RD
B	Date: Tuesday, March 19, 2019	Sheet 5 of 103

## CFG

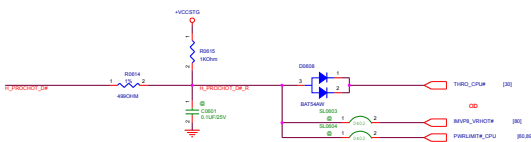


DDR VTT CTRL:  
System Memory Power Gate Control:  
Disables the platform memory VTT regulator  
in CH and deasserts and S3.  
Ref: Intel 570805\_Coffealake\_EDS\_Vol\_1\_Rev1.5 P.116

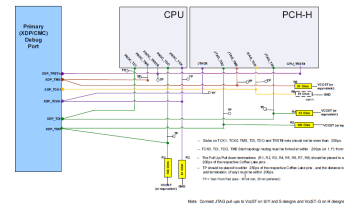
## VTT Enable



## CPU SIDEBAND SIGNALS



## Main Board



## CFG Straps for Processor

ref: Intel 570805\_Coffealake\_EDS\_Vol\_1\_Rev1.4 P.121

### CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted

- 1: (Default) Normal Operation, No stall
- 0: Stall

### CFG[1]: Reserved Configuration Lane

Reserved Configuration Lane

### CFG[2]: PCI Express® Static xE Lane Numbering Reversal

- 1: (Default) Normal Operation
- 0: Lane Numbers Reversed

### CFG[3]: Reserved configuration lanes

Reserved Configuration Lane

### CFG[4]: eOP Enable

- 1: Enabled
- 0: Disabled

### CFG[6-8]: PCI Express® Bifurcation

- 00: 1 x8, 2 x4 PCI Express®
- 01: Reserved
- 10: 2 x8 PCI Express®
- 11: 1 x8 PCI Express®

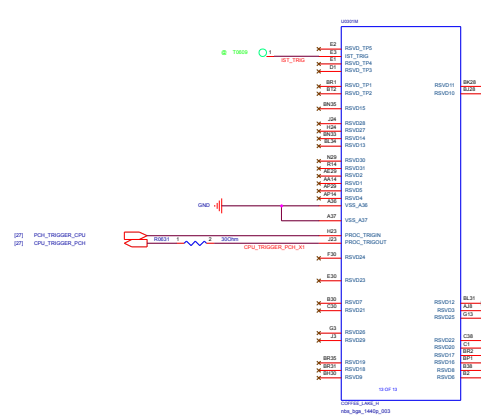
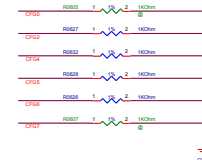
### CFG[7]: PEG Training

- 1: (Default) PEG Train Immediately Following RESET# de-assertion
- 0: PEG Wait for BIOS for Training

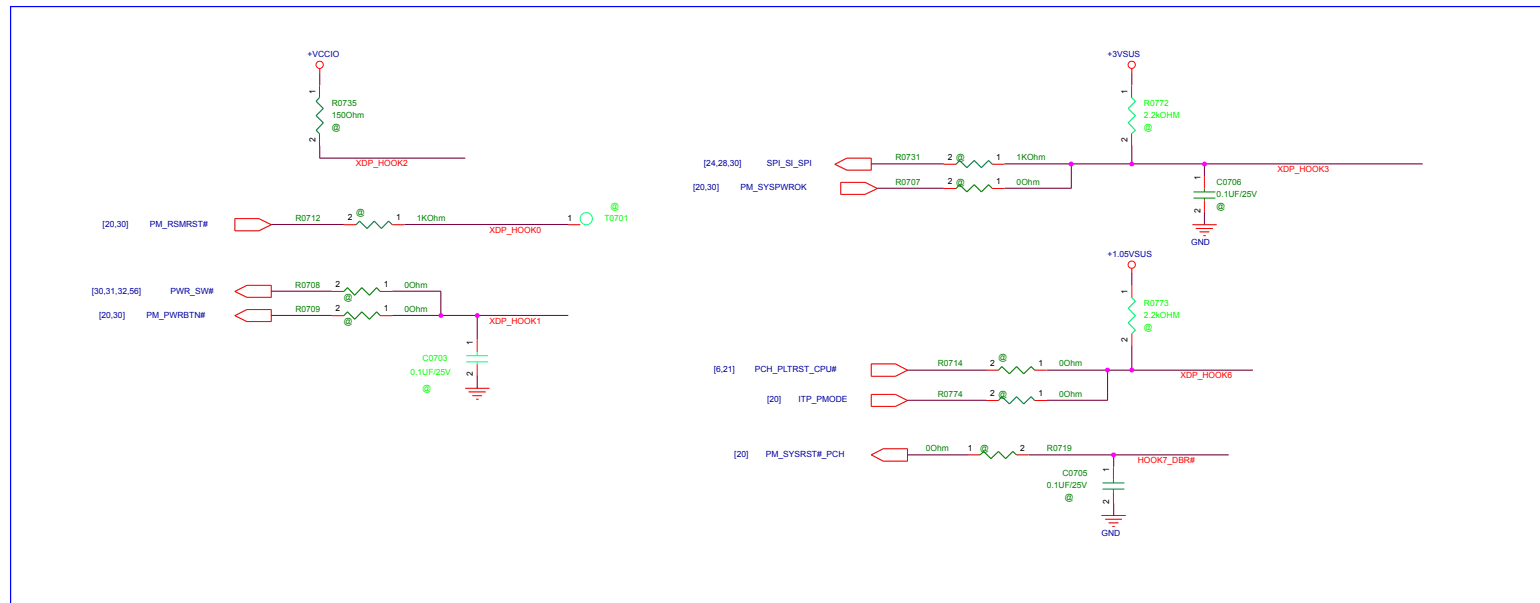
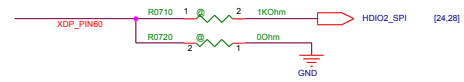
### CFG[19-8]: Reserved Configuration Lanes

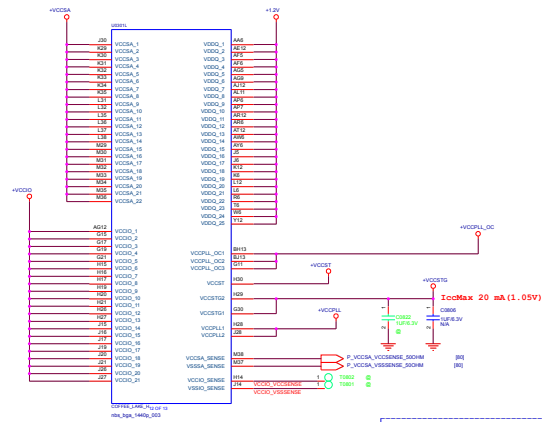
Reserved Configuration Lanes

## CFG Straps



ASUS		Project Name	Rev
G711GW			1.0
Title : CPU_CFG_REV0			
Rev	Dept.	Engineer	
C	ASUSTW COMPUTER	Gaming RD	
Date	Thursday, March 15, 2018	Time	6 of 103





Main Source	1th PWR	2nd PWR	3rd PWR
	+1.05VSBUS	+VCCSTG	
AC_BAT_SYS	+1.2V	+VCCSTG	
	+VCCSA	+VCCPLL_OC	
	+VCCIO	+VCCSTG	

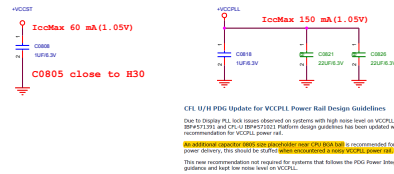
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFI H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected Soc power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

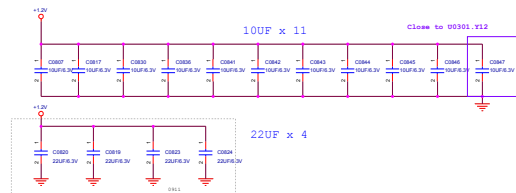
**CPU\_C10\_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL\_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.**

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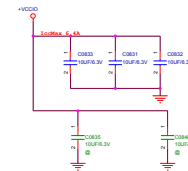
+VCCSTG/+VCCPLL  
DECAPS Place Back Side (TOP)



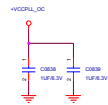
+VDDQ DECAPS Place Back Side (TOP)



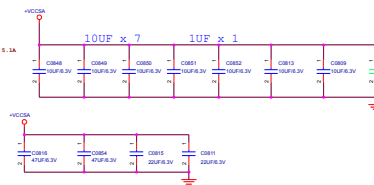
+VCCIO DECAPS Place Back Side (TOP)



+VCCPLL\_OC DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)

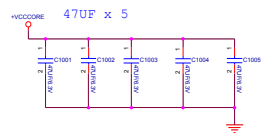


+VCCSA near CPU

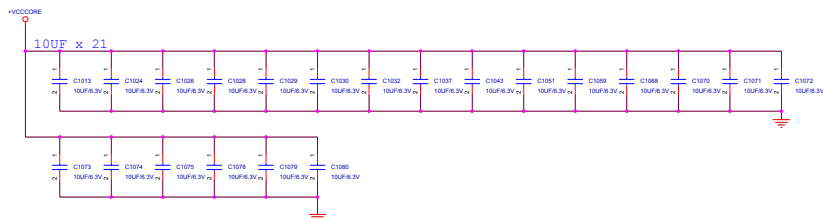
ASUS	Project Name	Rev
711GW		1.0
TYPE : CPU_PWR		
Set	Dept. : ASUS/CM/PC/EC	Engineer : Gaming RD
Doc. Version: March 18, 2019	Drawn	8



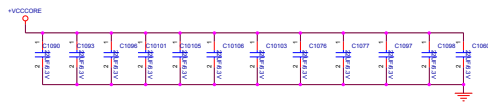
+VCCORE near CPU



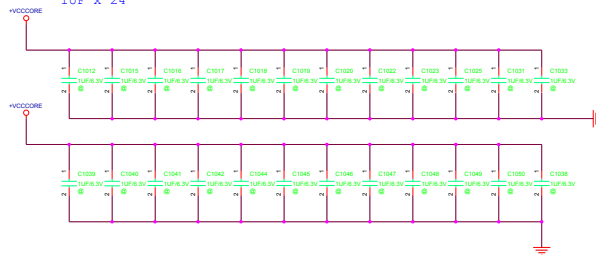
+VCCORE DECAPS Place Back Side (TOP)



22uF x 12



1uF x 24



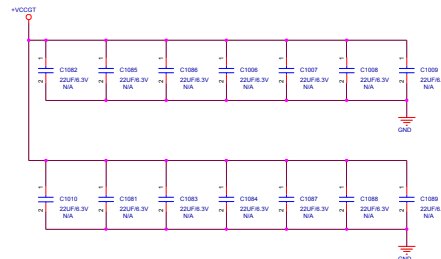
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
VCCGT	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

Main Board

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+VCCGT cap near CPU

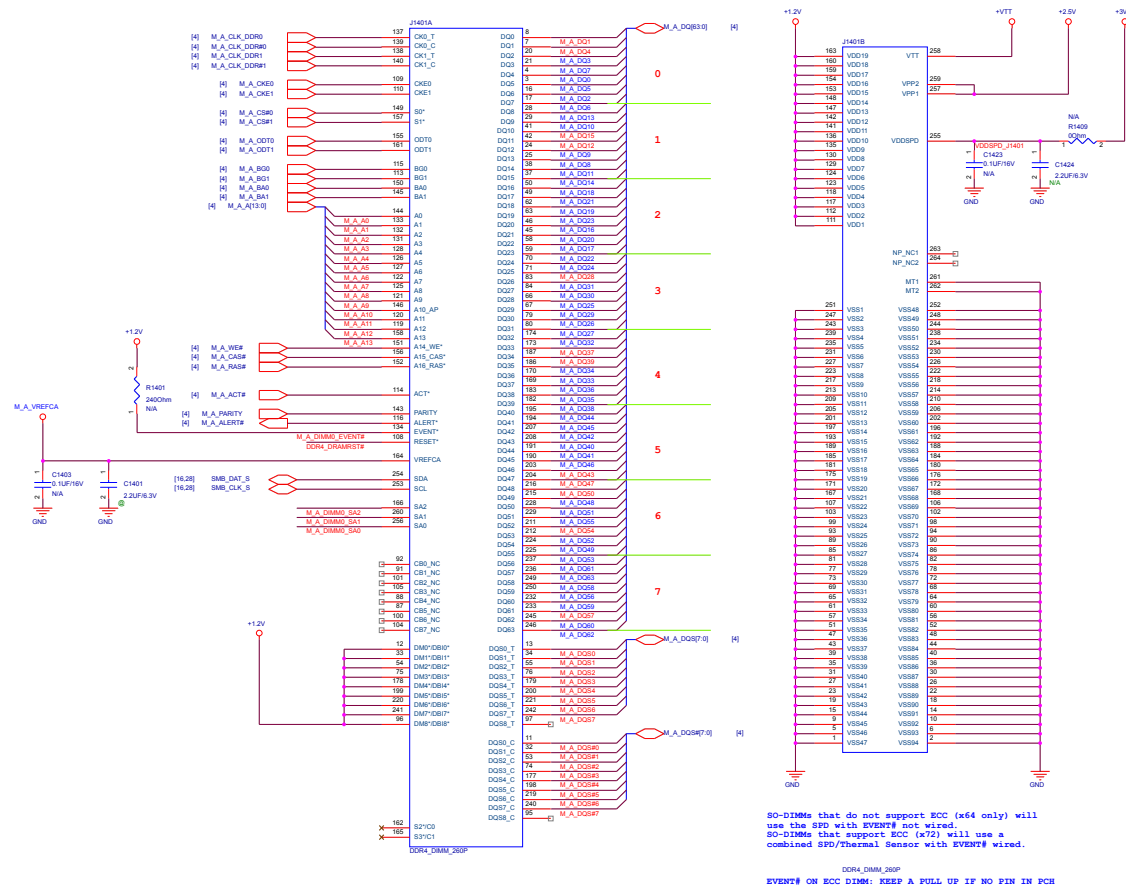
22uF x14



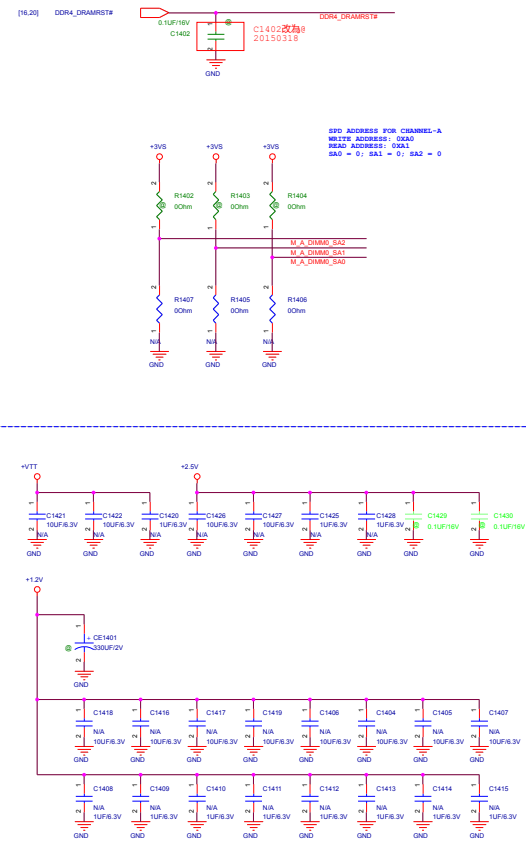
ASUS		Project Name	Rev
G711GW			1.0
Title : 610 CPU POWER CAP			
Size	Dept.:	ASUSNAK COMPUTER	Engineer: Gaming RD
Date: Tuesday, March 19, 2019			Sheet 10 of 103


Chris

SODIMM CHA-DIMM0  
TOP H4.0mm REV (J1401)

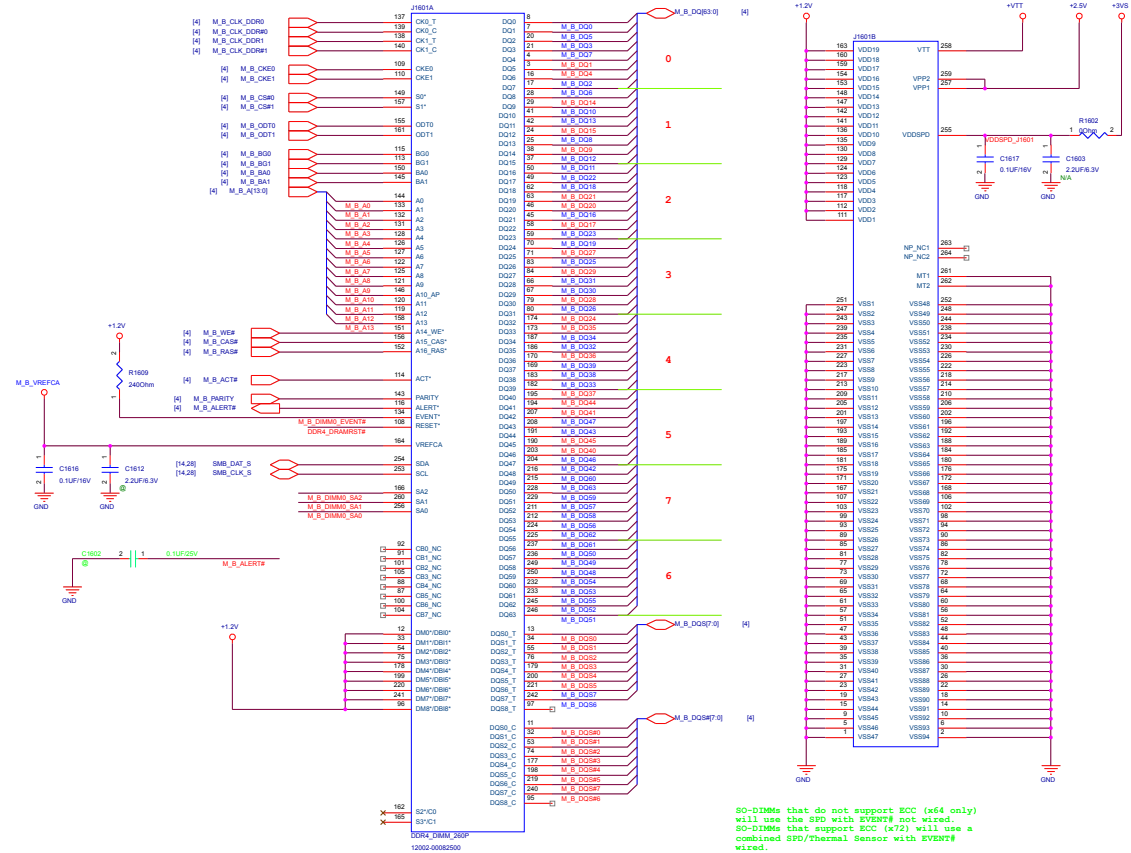


## Main Board



		Project Name <b>G711GW</b>		Rev <b>R1.0</b>
Title : <b>DIM_DDR4 SO-DIMM A1</b>				
Size Custom	Dept.: <b>ASUSTeK COMPUTER</b>		Engineer: <b>Gaming RD</b>	
Date: <b>Tuesday, March 19, 2019</b>		Sheet <b>14</b>	of <b>103</b>	

SODIMM CHB-DIMM0  
TOP H4.0mm STD (J1601)



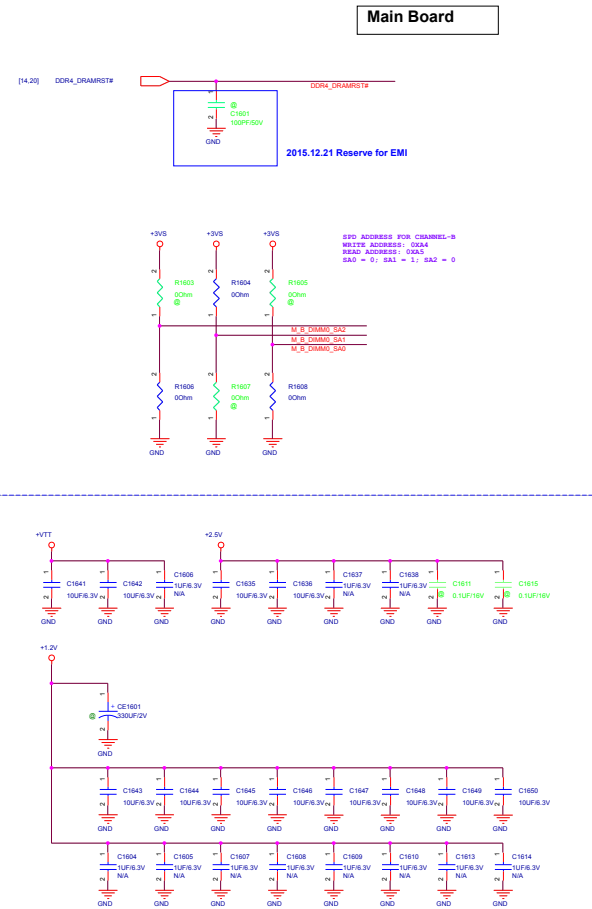
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.  
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

DDR4\_DIMM\_260F

```

EVENT# ON ECC DIMM: KERR-008501

```




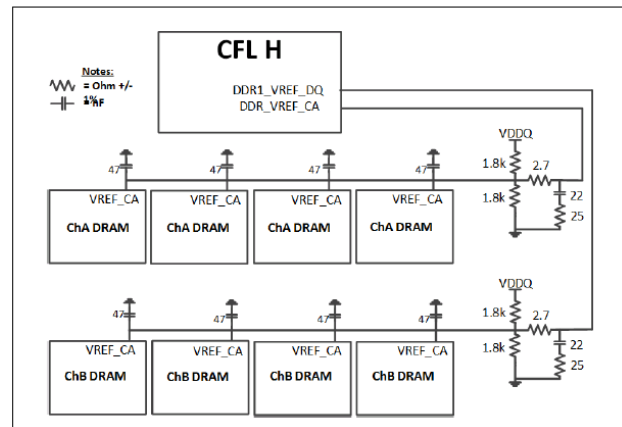
		Project Name <b>G711GW</b>		Rev <b>1.0</b>
Title : <b>DIM_DDR4 SO-DIMM B1</b>				
Size Custom	Dept.: <b>ASUSTek COMPUTER</b>		Engineer: <b>Gaming RD</b>	
Date: <b>Tuesday, March 19, 2019</b>		Sheet	<b>16</b>	of 103



Figure 4-23. CFL H DDR4 x16 Memory Down V<sub>REF-CA</sub> Overview



Vref for CHA\_DIMM0

Main Board

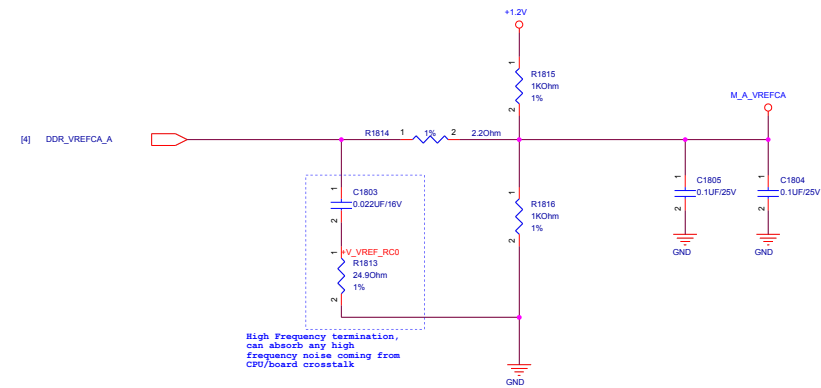
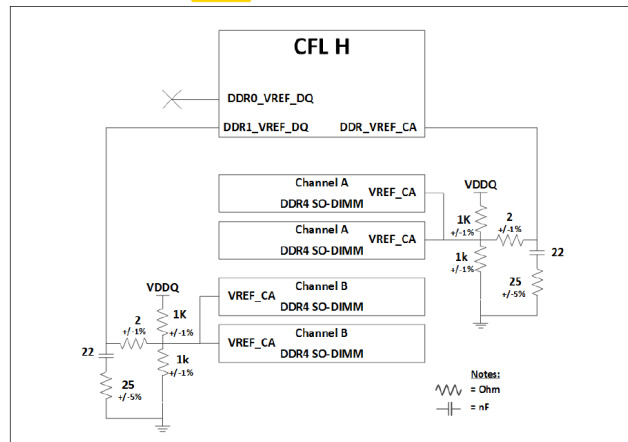
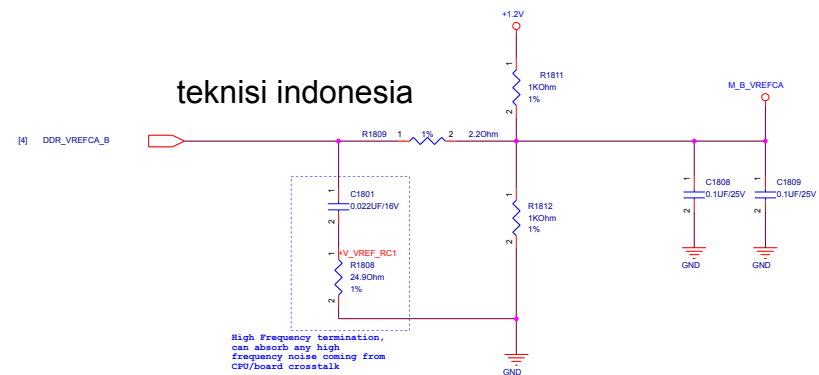


Figure 4-22. CFL-H DDR4 SO-DIMM V<sub>REF-CA</sub> Overview

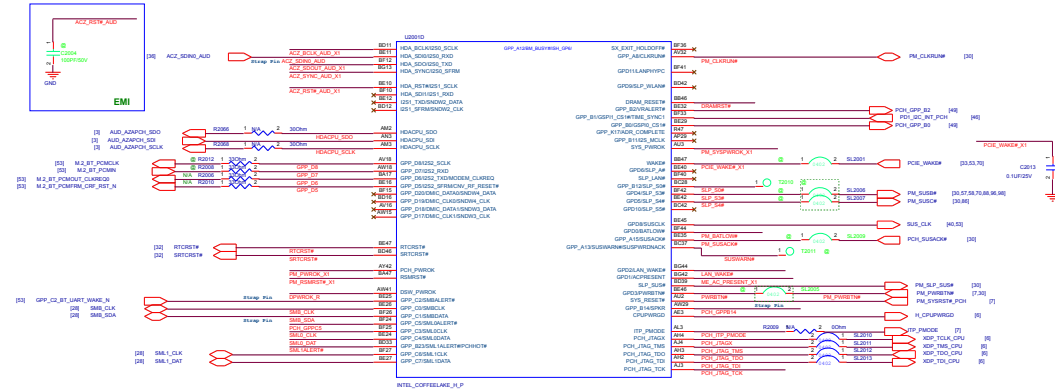


Vref for CHB\_DIMM0

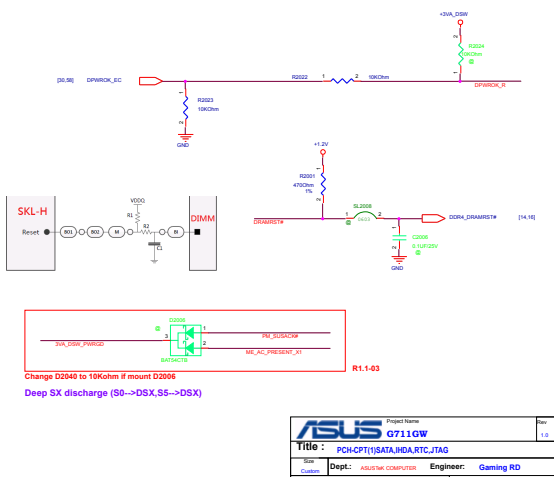
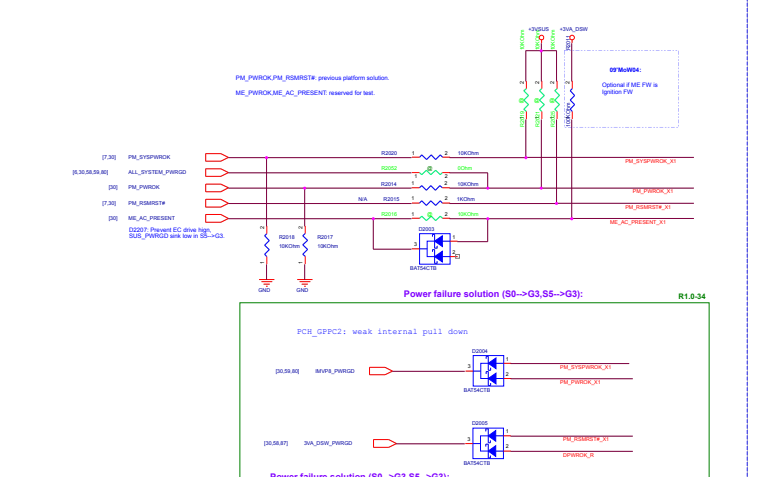
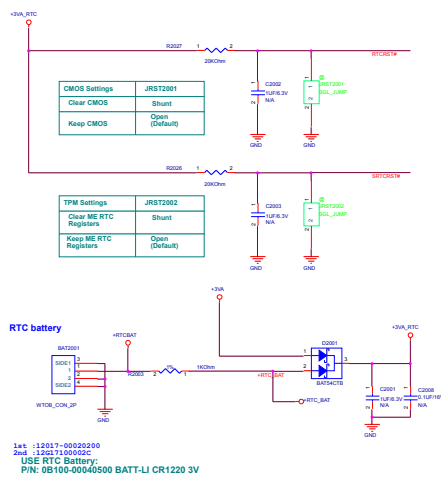
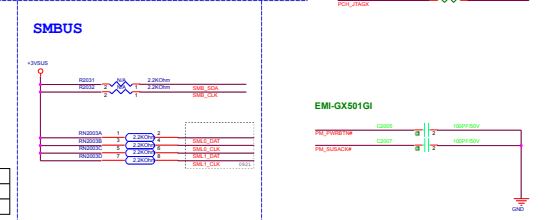
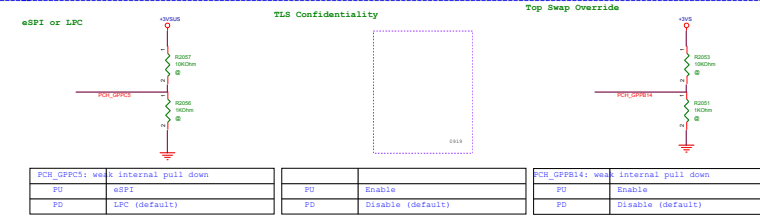


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ASUS		Project Name	Rev
G711GW			1.0
Title : DIM_CA/DQ Voltage			
Size	Dept.: ASUSTek COMPUTER	Engineer: Gaming RD	
B	Date: Tuesday, March 19, 2019	Sheet 18 of 103	

[illegible]

Main Source	1th FWR	2nd FWR	3rd FWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
		+3VSUS	+3VSUS_PCH	+V2_3A_VT_BA_VCCM20
	+3VA_DW	+3VS		



GX501GI PCIE/SATA Function define  
CNL HM370

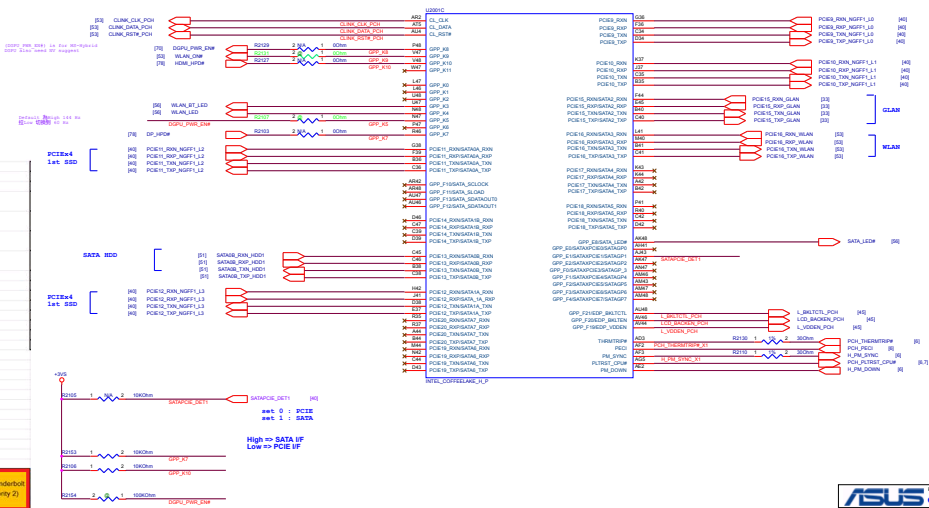
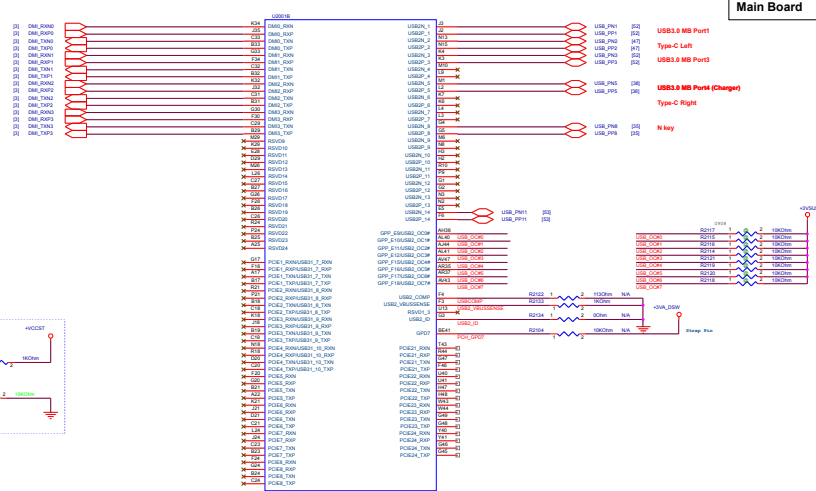
ISIO Capabilities	Function		Function
PCIe0 (From GPU)			GPU
PCIe#01 - USB3.1x807			CLKREQ_1
PCIe#02 - USB3.1x08			CLKREQ_2
PCIe#03 - USB3.1x09			CLKREQ_3
PCIe#04 - USB3.1x10			CLKREQ_4
PCIe#05			CLKREQ_5
PCIe#06			CLKREQ_6
PCIe#07			CLKREQ_7
PCIe#08			CLKREQ_8
PCIe#09			CLKREQ_9
PCIe#10	PCIe*4 SSD		CLKREQ_10-15
PCIe#11 - SATA-0a			
PCIe#12 - SATA-1a			
PCIe#13 - SATA-0b			
PCIe#14 - SATA-1b			
PCIe#15 - SATA#2			
PCIe#16 / SATA#3	WLAN		
PCIe#17 / SATA#4			
PCIe#18 / SATA#5			
PCIe#19 / SATA#6			
PCIe#20 / SATA#6			
PCIe#21	TBT (x4)		
PCIe#22			
PCIe#23			
PCIe#24			



## GX501GI USB Function define

USB 2.0	Function	USB 3.0	Function
US2R_01	USB3.0 MB Port	USB3_1A01	USB3.1MB Port1 (Support Gen2)
US2R_02	USB3.0 MB Port2	USB3_1A02	USB3.0 MB Port1 (Support Gen2)
US2R_03	USB3.0 MB Port3	USB3_1A03	USB3.0 MB Port1 (Support Gen2)
US2R_04	Camera	USB3_1A04	USB3.0 MB Port4 (Support Gen2)
US2R_05	USB3.0 MB Port4(Charger)	USB3_1A05	
US2R_06	TBT	USB3_1A06	
US2R_07		USB3_1A07	
US2R_08		USB3_1A08	
US2R_09	N key		
US2R_10	BT		
US2R_11			
US2R_12			

ID#0	FM370	QM370	CM245	IFB1	Devices Assign
0	USB3 1 Gen1/Gen2 #1	USB3 1 Gen1/Gen2 #1	USB3 1 Gen1/Gen2 #1	USB3 1 Gen1/Gen2 #1	port0 USB3 1 Type-C
1	USB3 1 Gen1/Gen2 #2	USB3 1 Gen1/Gen2 #2	USB3 1 Gen1/Gen2 #2	USB3 1 Gen1/Gen2 #2	port1 USB3 1 Type-C
2	USB3 1 Gen1/Gen2 #3	USB3 1 Gen1/Gen2 #3	USB3 1 Gen1/Gen2 #3	USB3 1 Gen1/Gen2 #3	port0 USB3 0 Type-A USB3 1 Type-A
3	USB3 1 Gen1/Gen2 #4	USB3 1 Gen1/Gen2 #4	USB3 1 Gen1/Gen2 #4	USB3 1 Gen1/Gen2 #4	port0 USB3 0 Type-A USB3 1 Type-A
4	USB3 1 Gen1 #5	USB3 1 Gen1/Gen2 #5	USB3 1 Gen1/Gen2 #5	USB3 1 Gen1/Gen2 #5	port0 USB3 0 Type-A USB3 1 Type-A
5	USB3 1 Gen1 #6	USB3 1 Gen1/Gen2 #6	USB3 1 Gen1/Gen2 #6	USB3 1 Gen1/Gen2 #6	port0 USB3 0 Type-A USB3 1 Type-A
6	USB3 1 Gen1 #7	USB3 1 Gen1 #7	USB3 1 Gen1 #7	USB3 1 Gen1 #7	port0 USB3 0 Type-A USB3 1 Type-A
7	USB3 1 Gen1 #8	USB3 1 Gen1 #8	USB3 1 Gen1 #8	USB3 1 Gen1 #8	port0 USB3 0 Type-A USB3 1 Type-A
8	NA	USB3 1 Gen1 #9	USB3 1 Gen1 #9	USB3 1 Gen1 #9	port0 USB3 0 Type-A USB3 1 Type-A
9	NA	USB3 1 Gen1 #10	USB3 1 Gen1 #10	USB3 1 Gen1 #10	port0 USB3 0 Type-A USB3 1 Type-A
10	NA	PCIE #1	PCIE #1	PCIE #1	port0 USB3 0 Type-A USB3 1 Type-A
11	NA	PCIE #2	PCIE #2	PCIE #2	port0 USB3 0 Type-A USB3 1 Type-A
12	NA	PCIE #3	PCIE #3	PCIE #3	port0 USB3 0 Type-A USB3 1 Type-A
13	NA	PCIE #4	PCIE #4	PCIE #4	port0 USB3 0 Type-A USB3 1 Type-A
14	PCIE #5	PCIE #5	PCIE #5	PCIE #5	port0 USB3 0 Type-A USB3 1 Type-A
15	PCIE #6	PCIE #6	PCIE #6	PCIE #6	port0 USB3 0 Type-A USB3 1 Type-A
16	PCIE #7	PCIE #7	PCIE #7	PCIE #7	port0 USB3 0 Type-A USB3 1 Type-A
17	PCIE #8	PCIE #8	PCIE #8	PCIE #8	port0 USB3 0 Type-A USB3 1 Type-A
18	PCIE #9	PCIE #9	PCIE #9	PCIE #9	port0 USB3 0 Type-A USB3 1 Type-A
19	PCIE #10	PCIE #10	PCIE #10	PCIE #10	port0 USB3 0 Type-A USB3 1 Type-A
20	PCIE #11	PCIE #11	PCIE #11	PCIE #11	port0 USB3 0 Type-A USB3 1 Type-A
21	PCIE #12	PCIE #12	PCIE #12	PCIE #12	port0 USB3 0 Type-A USB3 1 Type-A
22	PCIE #13	PCIE #13	PCIE #13	PCIE #13	port0 USB3 0 Type-A USB3 1 Type-A
23	PCIE #14	PCIE #14	PCIE #14	PCIE #14	port0 USB3 0 Type-A USB3 1 Type-A
24	PCIE #15	PCIE #15	PCIE #15	PCIE #15	port0 USB3 0 Type-A USB3 1 Type-A
25	PCIE #16	PCIE #16	PCIE #16	PCIE #16	port0 USB3 0 Type-A USB3 1 Type-A
26	PCIE #17	PCIE #17	PCIE #17	PCIE #17	port0 USB3 0 Type-A USB3 1 Type-A
27	PCIE #18	PCIE #18	PCIE #18	PCIE #18	port0 USB3 0 Type-A USB3 1 Type-A
28	PCIE #19	PCIE #19	PCIE #19	PCIE #19	port0 USB3 0 Type-A USB3 1 Type-A
29	PCIE #20	PCIE #20	PCIE #20	PCIE #20	port0 USB3 0 Type-A USB3 1 Type-A
30	PCIE #21	PCIE #21	PCIE #21	PCIE #21	port0 USB3 0 Type-A USB3 1 Type-A
31	PCIE #22	PCIE #22	PCIE #22	PCIE #22	port0 USB3 0 Type-A USB3 1 Type-A
32	PCIE #23	PCIE #23	PCIE #23	PCIE #23	port0 USB3 0 Type-A USB3 1 Type-A
33	PCIE #24	PCIE #24	PCIE #24	PCIE #24	port0 USB3 0 Type-A USB3 1 Type-A
34	PCIE #25	PCIE #25	PCIE #25	PCIE #25	port0 USB3 0 Type-A USB3 1 Type-A
35	PCIE #26	PCIE #26	PCIE #26	PCIE #26	port0 USB3 0 Type-A USB3 1 Type-A
36	PCIE #27	PCIE #27	PCIE #27	PCIE #27	port0 USB3 0 Type-A USB3 1 Type-A
37	PCIE #28	PCIE #28	PCIE #28	PCIE #28	port0 USB3 0 Type-A USB3 1 Type-A
38	PCIE #29	PCIE #29	PCIE #29	PCIE #29	port0 USB3 0 Type-A USB3 1 Type-A
39	PCIE #30	PCIE #30	PCIE #30	PCIE #30	port0 USB3 0 Type-A USB3 1 Type-A
40	PCIE #31	PCIE #31	PCIE #31	PCIE #31	port0 USB3 0 Type-A USB3 1 Type-A
41	PCIE #32	PCIE #32	PCIE #32	PCIE #32	port0 USB3 0 Type-A USB3 1 Type-A
42	PCIE #33	PCIE #33	PCIE #33	PCIE #33	port0 USB3 0 Type-A USB3 1 Type-A
43	PCIE #34	PCIE #34	PCIE #34	PCIE #34	port0 USB3 0 Type-A USB3 1 Type-A
44	PCIE #35	PCIE #35	PCIE #35	PCIE #35	port0 USB3 0 Type-A USB3 1 Type-A
45	PCIE #36	PCIE #36	PCIE #36	PCIE #36	port0 USB3 0 Type-A USB3 1 Type-A
46	PCIE #37	PCIE #37	PCIE #37	PCIE #37	port0 USB3 0 Type-A USB3 1 Type-A
47	PCIE #38	PCIE #38	PCIE #38	PCIE #38	port0 USB3 0 Type-A USB3 1 Type-A
48	PCIE #39	PCIE #39	PCIE #39	PCIE #39	port0 USB3 0 Type-A USB3 1 Type-A
49	PCIE #40	PCIE #40	PCIE #40	PCIE #40	port0 USB3 0 Type-A USB3 1 Type-A
50	PCIE #41	PCIE #41	PCIE #41	PCIE #41	port0 USB3 0 Type-A USB3 1 Type-A
51	PCIE #42	PCIE #42	PCIE #42	PCIE #42	port0 USB3 0 Type-A US



[illegible]

For Optimus

CLK\_PEGA\_RECV

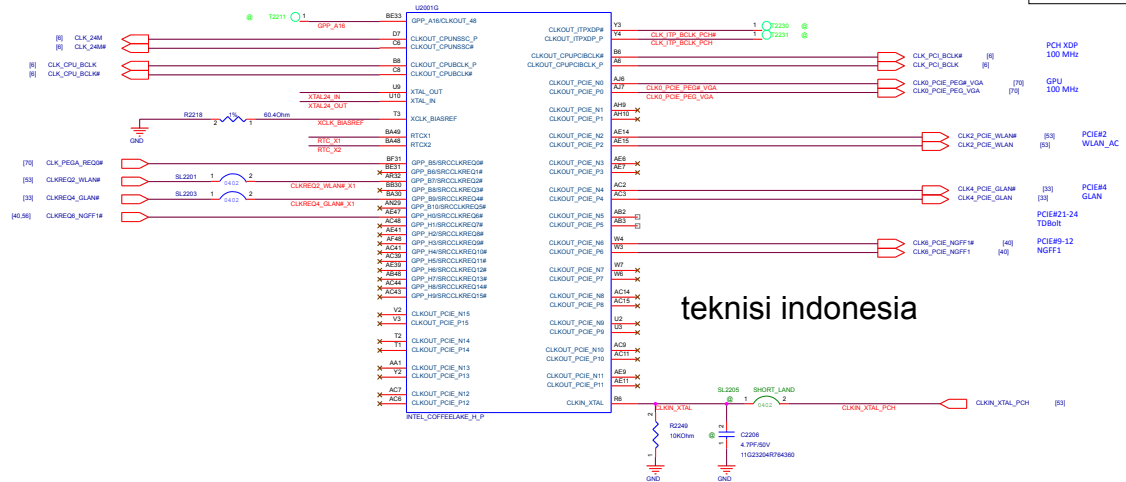
R2203  
10KOhm

Q2201  
2N7002K  
N/A

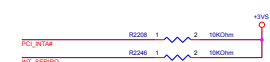
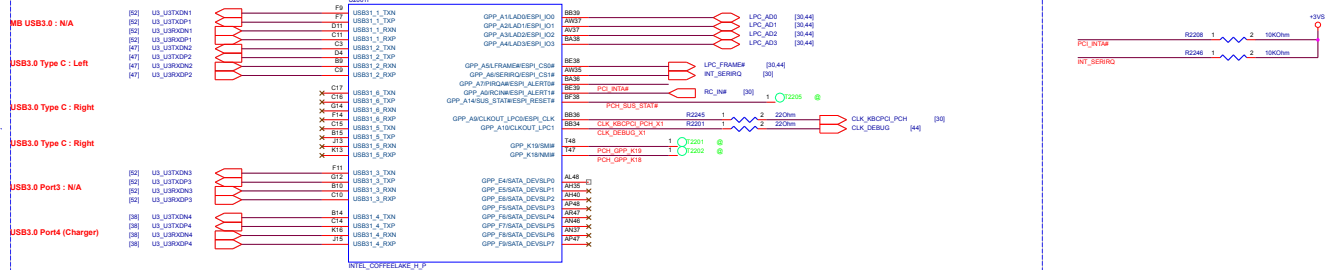
DGPU\_PWRON (P5, 70, 77)

GND

The diagram illustrates the electrical connection for the CLKREQ# signal in an Intel SSD. It shows two main signal paths originating from a +3V3BUS supply. The first path includes resistors R2203 and R2215, followed by a 100 Ohm termination resistor, and then splits into two parallel lines labeled CLKREQ#\_WLANK\_X1 and CLKREQ#\_GLANK\_X1. The second path includes resistor R2223 and a 100 Ohm termination resistor, leading to the CLK\_REQ#\_REQ2Q# pin. A second section, separated by a dashed line, shows a similar path for Intel SSD leakage, starting from a +3V3 supply, passing through resistor R2217 and a 100 Ohm termination resistor, and ending at the CLKREQ#\_NOFF\_1# pin.



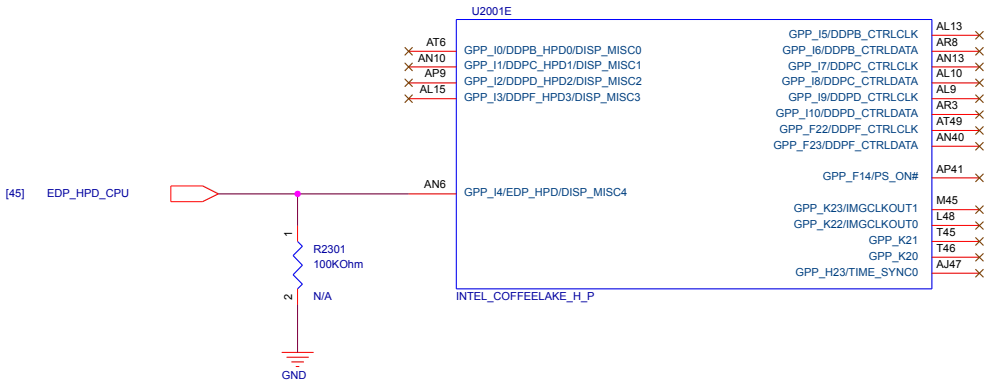
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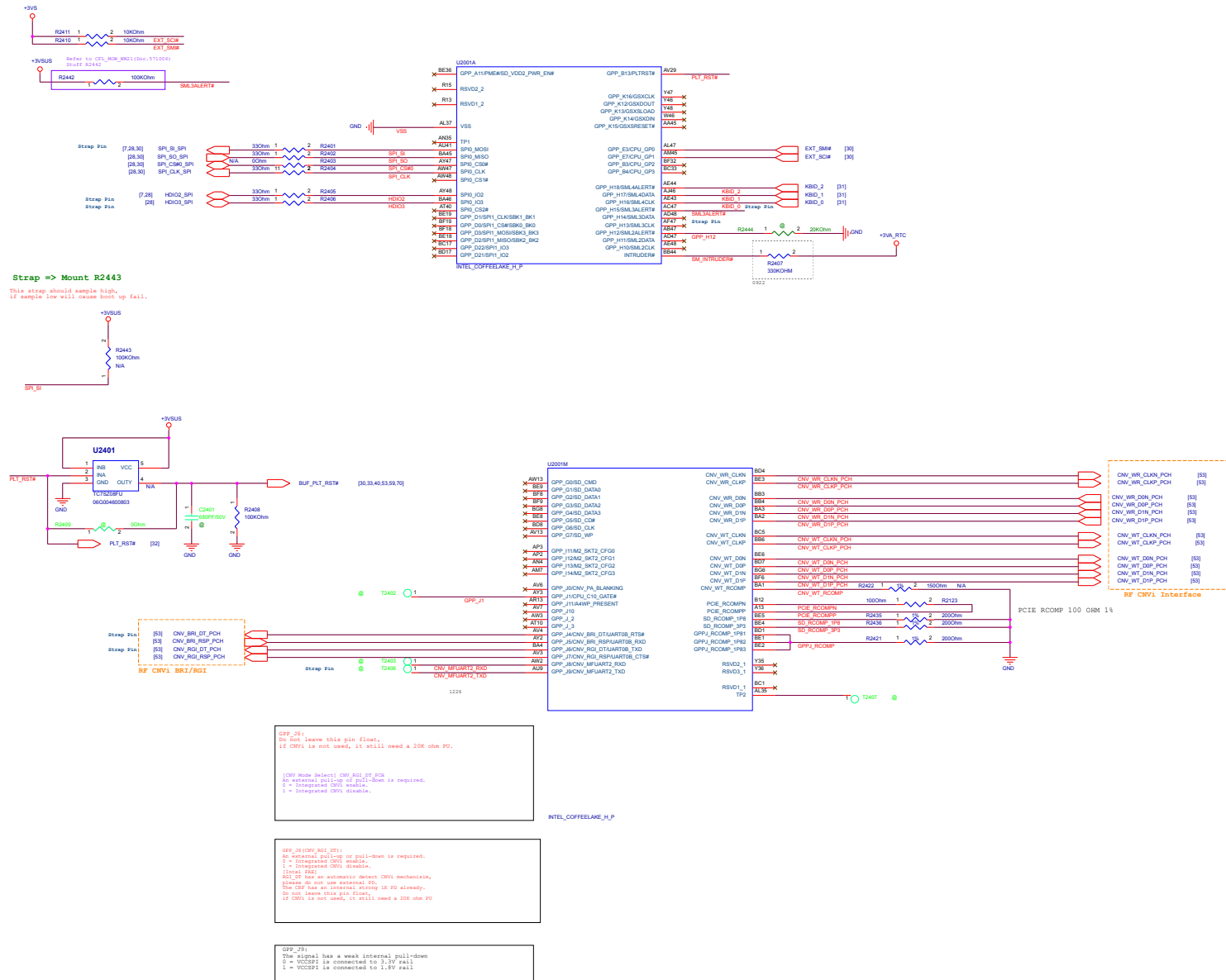


Main Board

- HPD0 to DP
- HPD1 to HDMI
- HPD2 to TBT
- HPD3 to VGA
- HPD4 to EDP Panel

DDP Strap Setting Update:  
0 = Port is not detected (Default)  
1 = Port is detected







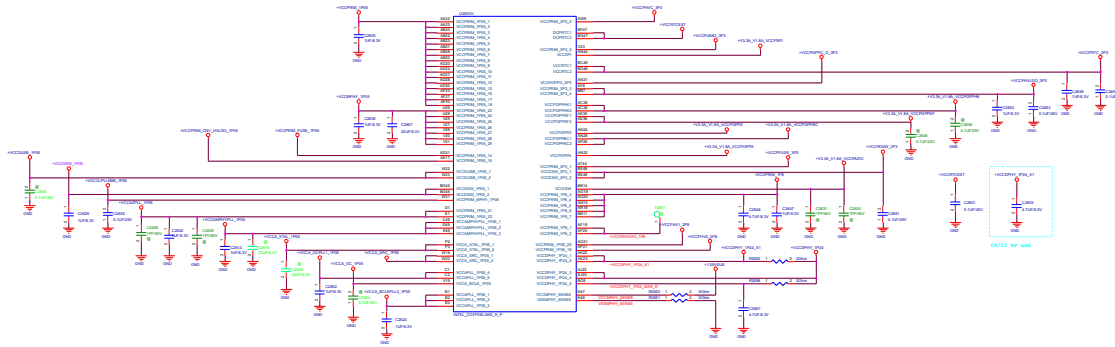
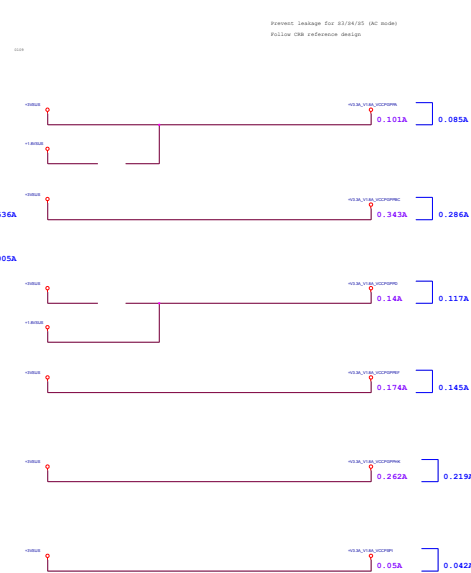
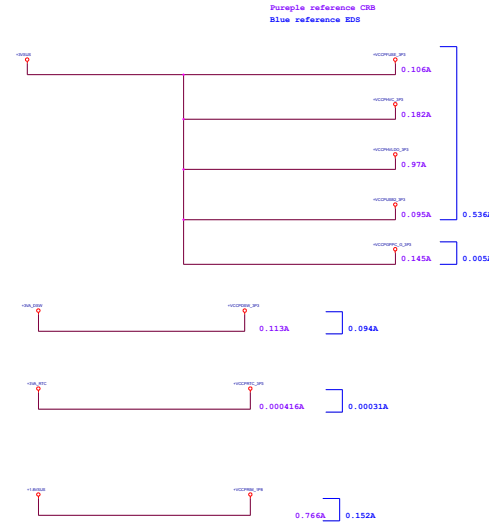
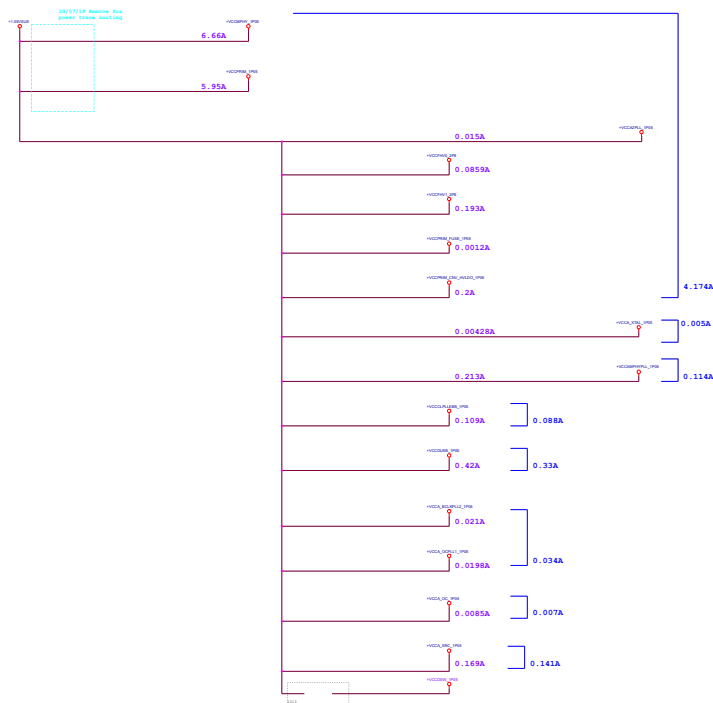


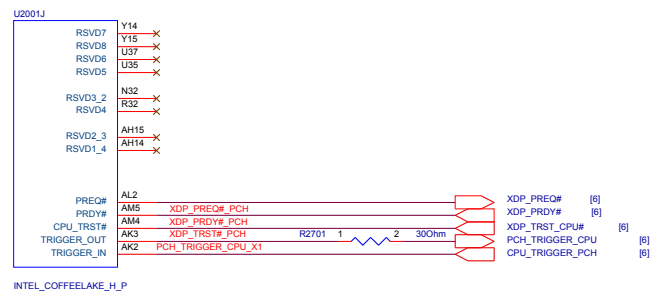
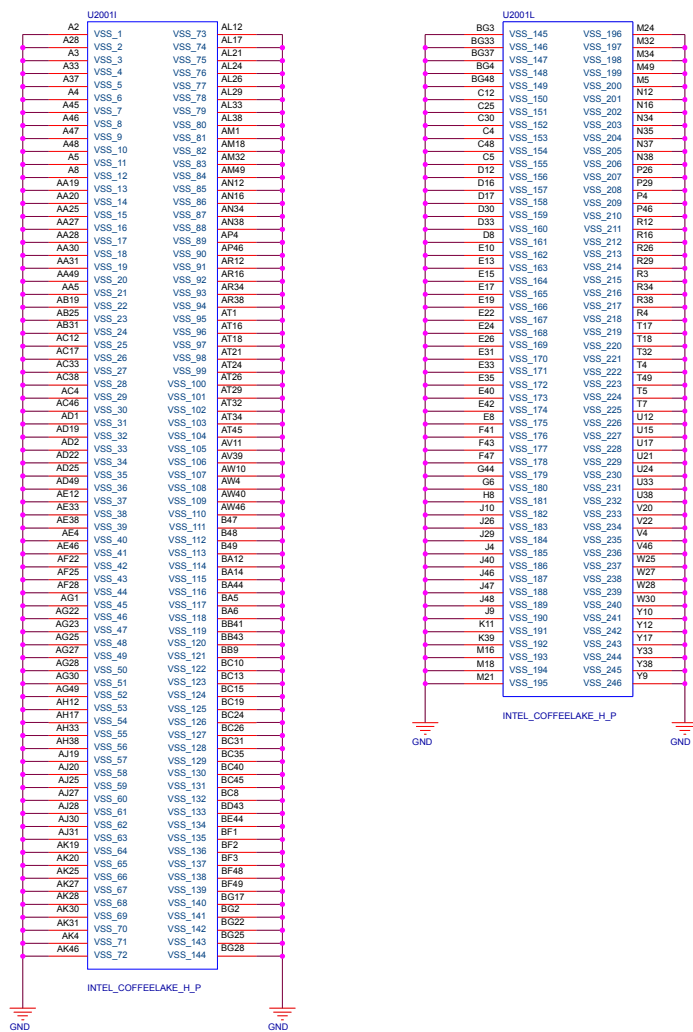
Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPCHVDDO_1PB	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPCHVDDO_1PB rail in Internal 1.8 v VDD Mode and left as no-connect in External 1.8V VDD Mode.
VCCPCHVDDO_1PB	1.8V or 3.3V for GPP_A group.
VCCPCHVDDO_1PB	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPCHVDDO_1PB	1.8V or 3.3V for GPP_D group.
VCCPCHVDDO_1PB	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPCHVDDO_1PB	3.3V for GPP_G group.
VCCPCHVDDO_1PB	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCPCHVDDO_1PB	1.8V Sense Line.
VSSPCHVDDO_1PB	0V (Ground) Sense Line.
VSS	Ground.



Present leakage for 82/84/85 (AC mode)  
Follow 100 reference design





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Project Name		Rev
ASUS G711GW		1.0
Title : PCH-CPT(8) POWER,GND		
Size	Dept.:	Engineer:
B	ASUSTek COMPUTER	Gaming RD
Date: Tuesday, March 19, 2019		Sheet 27 of 103

# SPI Power

[illegible]

# System Management Interface

The diagram illustrates the System Management Interface (SMI) connections between the Platform Controller Hub (PCH) and the Embedded Controller (EC). The PCH block is shown at the top, featuring signals SMB1\_CLK and SMB1\_DAT, and power supplies +12VS, +3VS, and +3.3V\_I0VDD. The EC block is shown at the bottom, featuring signals SMB3\_CLK and SMB3\_DAT, and a +3.3V\_I0VDD power supply. The diagram includes various components such as EMBAK1-G-T2R, Q2803A, Q2803B, Q2804A, Q2804B, RN2802B, RN2802A, RN2803B, and RN2803A.

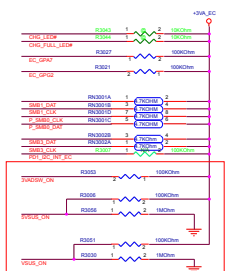
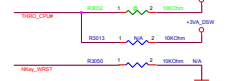
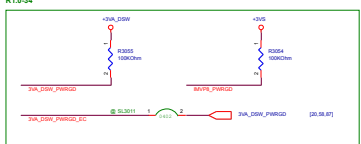
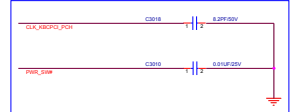
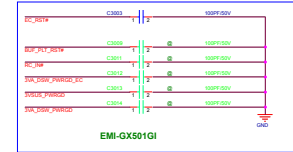
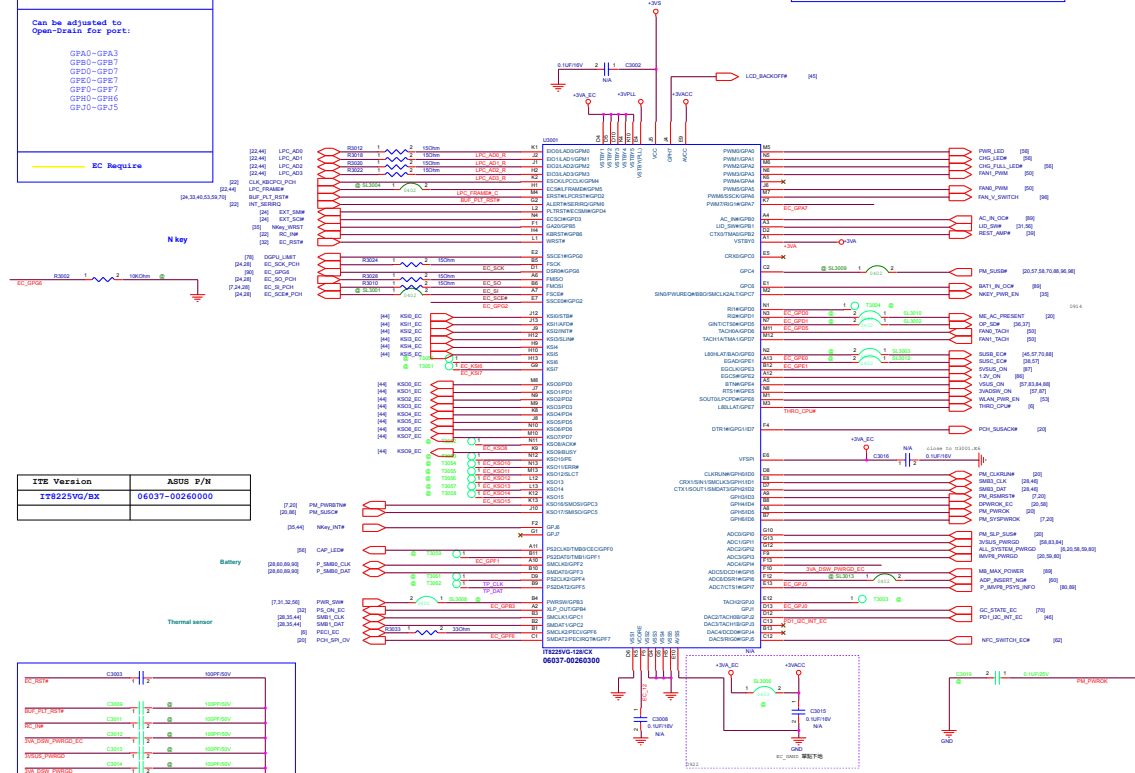
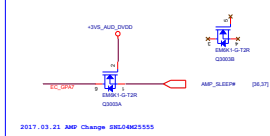
### SMBus Interface

The diagram illustrates the SMDbus interface for the PC8101A. It shows a PCB with two connectors, PC8101A and PC8101B. The PC8101A connector has pins 9 and 10, which are connected to the SMDbus\_CLK and SMDbus\_SDA lines, respectively. The PC8101B connector has pins 9 and 10, which are connected to the SMDbus\_CLK and SMDbus\_SDA lines, respectively. The SMDbus\_CLK line is connected to a 12V5S power supply through a 4.7KOhm resistor. The SMDbus\_SDA line is connected to a 12V5S power supply through a 4.7KOhm resistor. The SMDbus interface is labeled as SMDbus\_CLK [14:16] and SMDbus\_SDA [14:16].

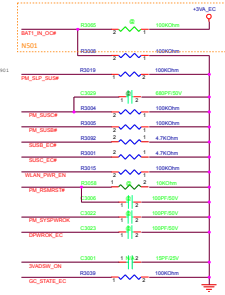
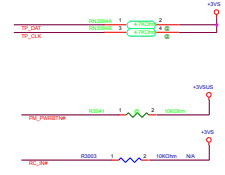


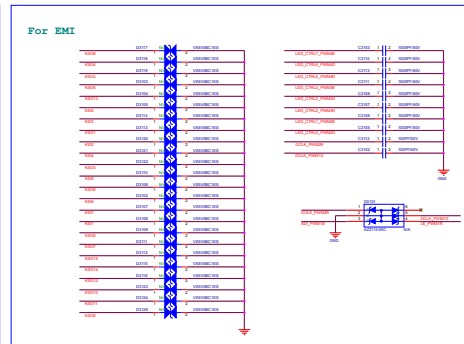
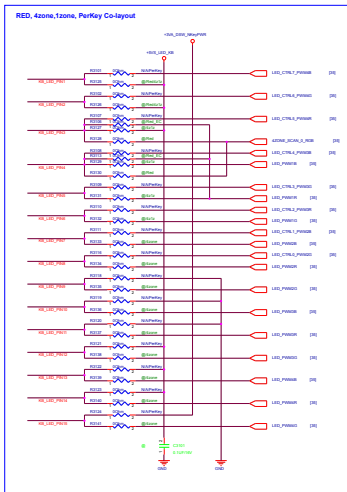
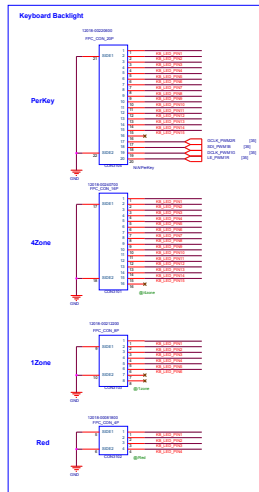
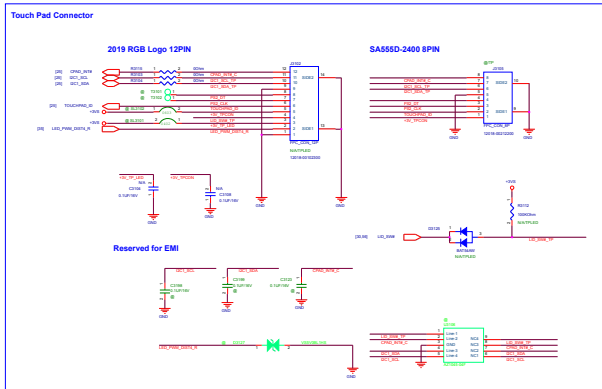
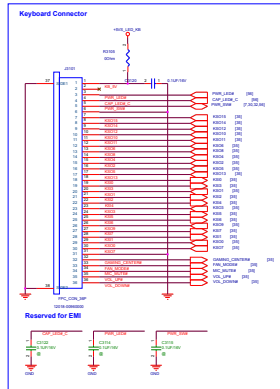
```
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
```

GPA0-GPA3  
GPB0-GPB7  
GPD0-GPD7  
GPE0-GPE7  
GPF0-GPF7  
GPH0-GPH6  
GPJ0-GPJ5



```
for load code
```





Keyboard ID



KB ID PCH Side(hw請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERTASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

	RED-4pin	1zone RGB_8pin	4zone-16pin	per key-20pin
pin1	VCC	VCC green	VCC green	COM7
pin2	VCC	VCC red	VCC red	COM6
pin3	GND	VCC blue	VCC blue	COM5
pin4	GND	LED1 blue	LED1 blue	COM4
pin5		LED1 red	LED1 red	COM3
pin6		LED1 green	LED1 green	COM2
pin7		NC	LED2 blue	COM1
pin8		NC	LED2 red	COM0
pin9			LED2 green	GND
pin10			LED3 blue	GND
pin11			LED3 red	GND
pin12			LED3 green	VCC
pin13			LED4 blue	VCC
pin14			LED4 red	VCC
pin15			LED4 green	VDD-33
pin16			NC	NC
pin17				GCLK
pin18				SDI
pin19				DCLK
pin20				LE

ASUS ROG Strix

Title: RGB KB & TP

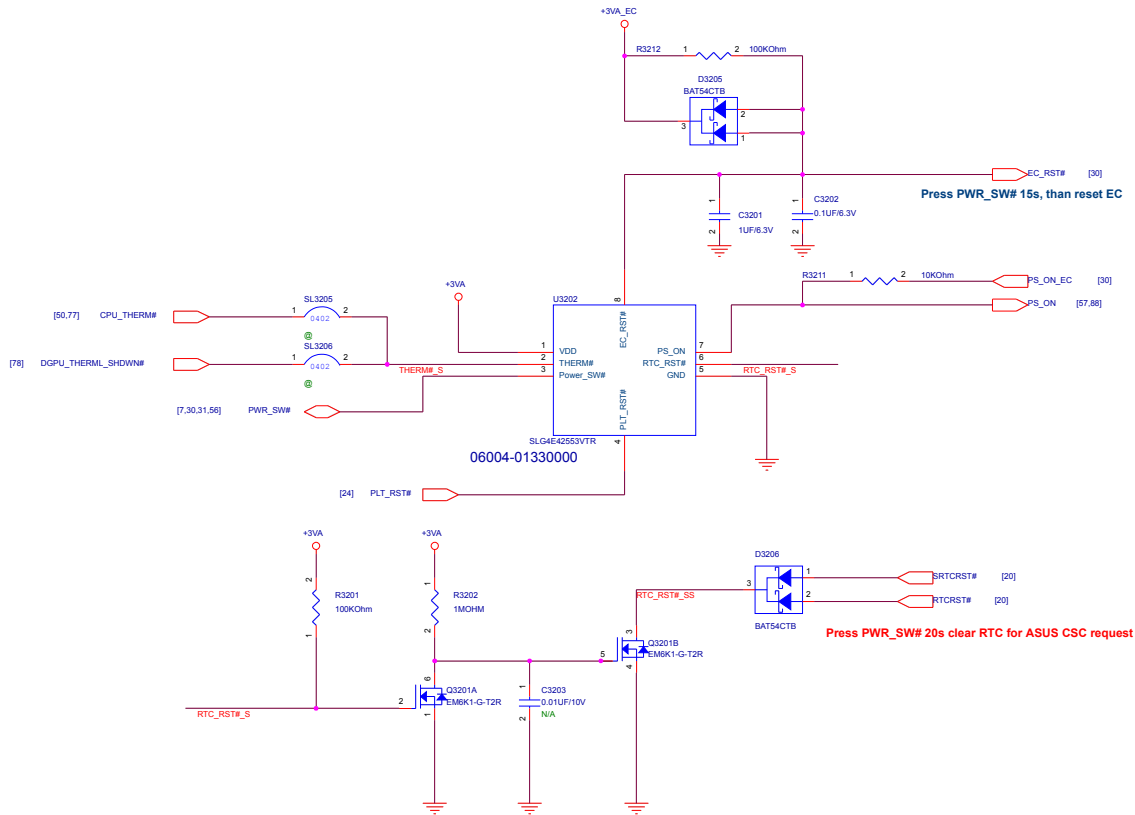
Drawn: ASUS ROG Strix

Engineer: Gaming RG

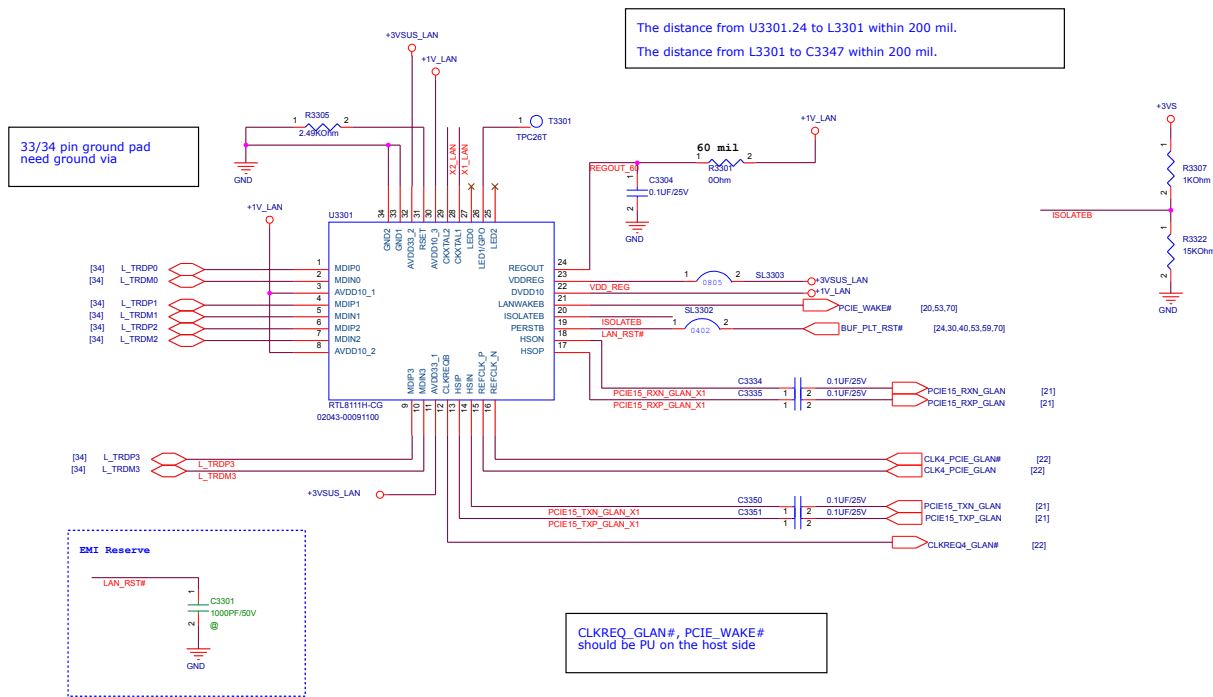
Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

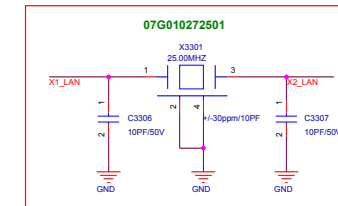
<https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components>  
UX362FA R1.3 board will verify this circuit 7/E



<Variant Name>		Title : RST_Reset Circuit	
ASUS		Engineer: Gaming RD	
Size	Project Name	Rev	
B	G711GW	1.0	
Date:	Tuesday, March 19, 2019	Sheet	32 of 103



## Main Board

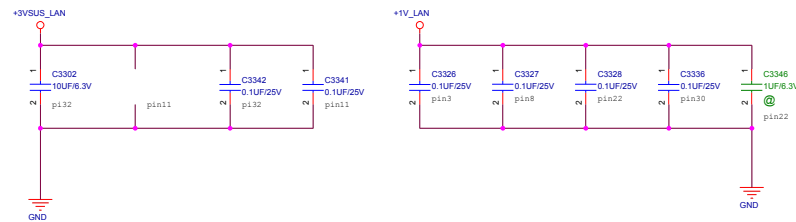
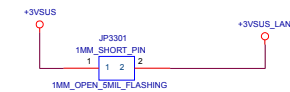


X3301: 25MHz +/-30ppm/10pF (3225)

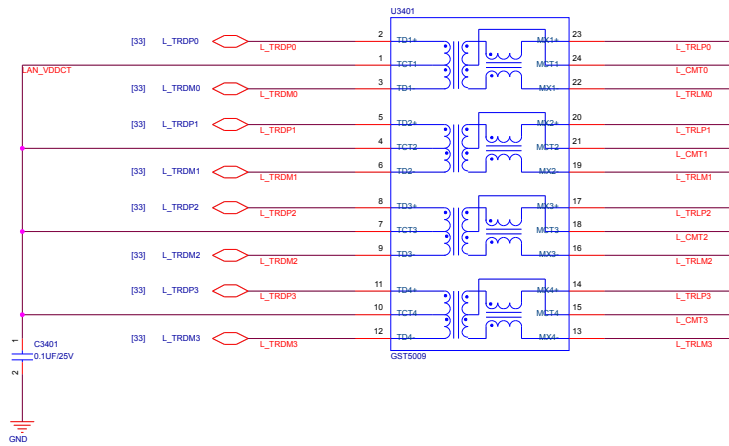
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

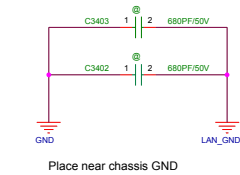
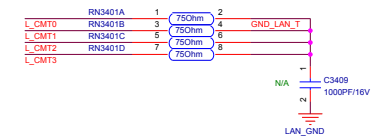
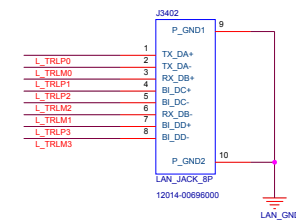
Realtek suggests 3V\_LAN raise time >1ms



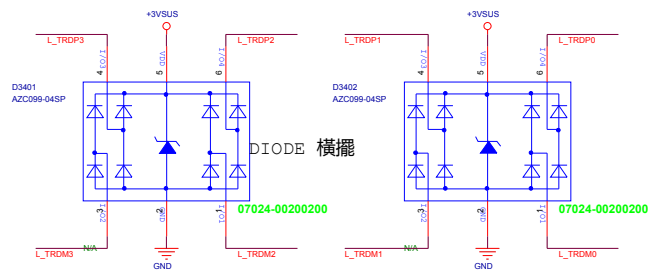
Project Name		Rev
ASUS GX502GX		1.0
Title : LAN RTL8111GUX-CG		
Size	Dept.:	Engineer:
B	ASUSTek COMPUTER	NB1 RD2 EE1
Date: Tuesday, March 19, 2019	Sheet	33 of 103



## LAN Connector

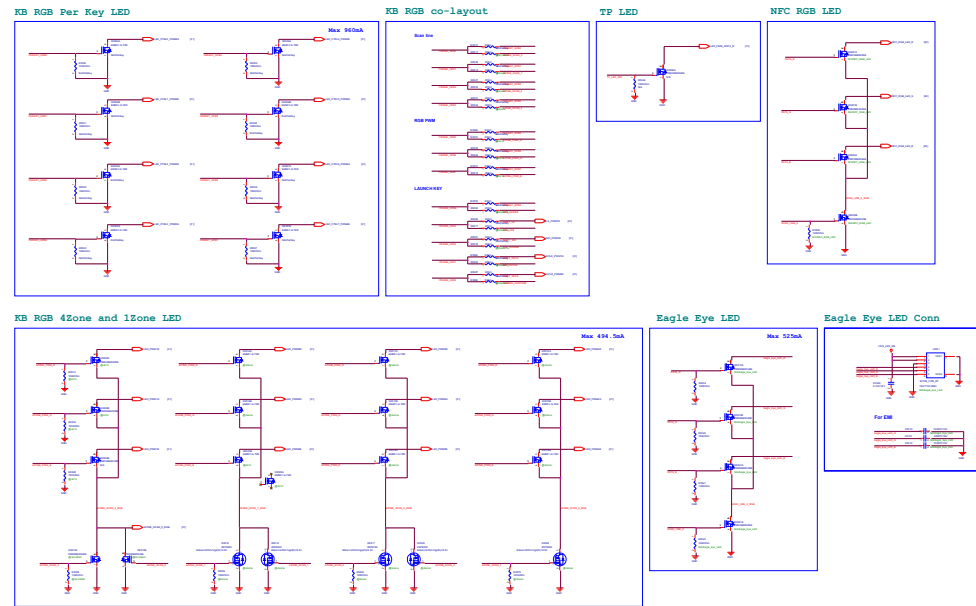
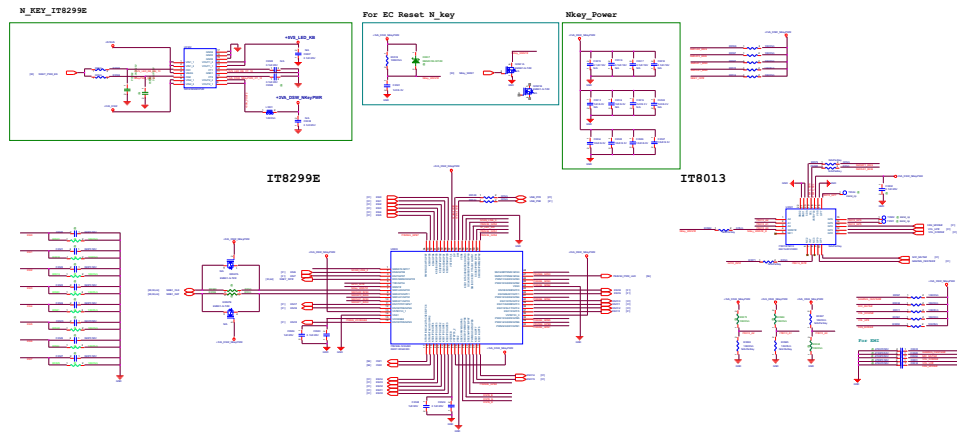


Place near chassis GND

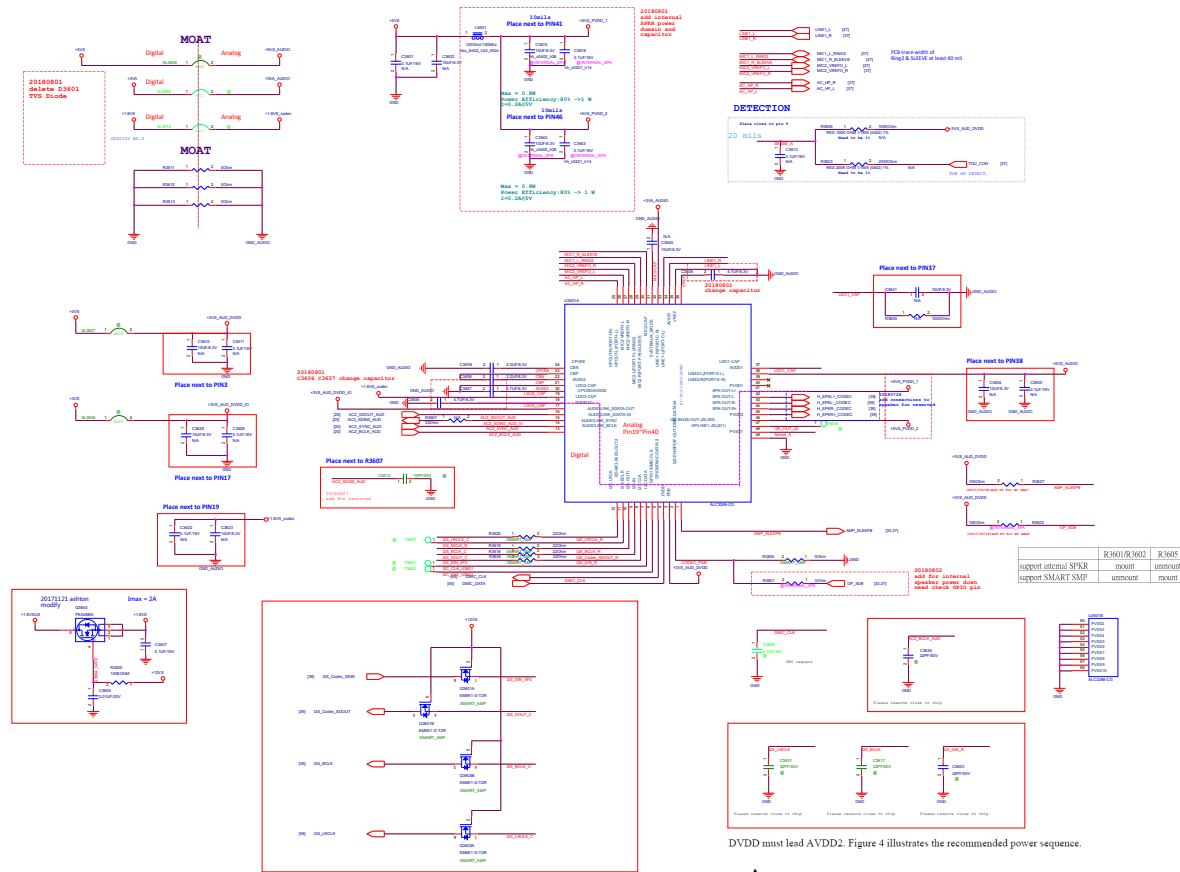


D3401, D3402 ESD Diode  
1st Source: P/N: 07024-00200200 AMAZING/AZC099-04SP.R7G  
2nd Source: P/N: 07024-00710000 NXP/PUSB2X4D

ASUS		Project Name	Rev
GX502GX			1.0
Title : LAN_RJ45_CON			
Size	Dept.:	ASUSTek COMPUTER	Engineer: NB1 RD2 EE1
C			
Date: Tuesday, March 19, 2019	Sheet	34	of 103







DVDD must lead AVDD2. Figure 4 illustrates the recommended power sequence.

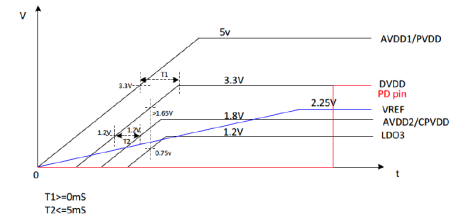
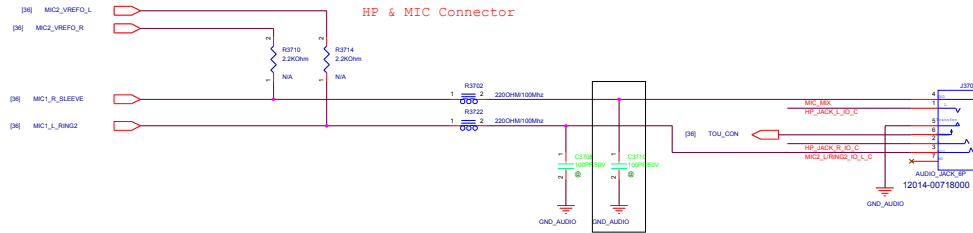
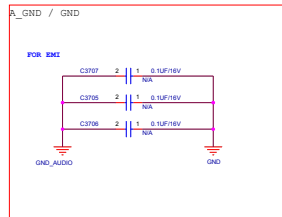


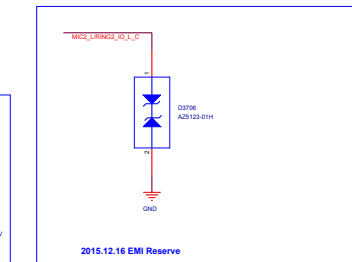
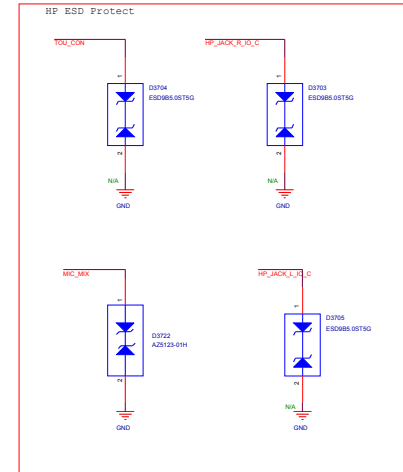
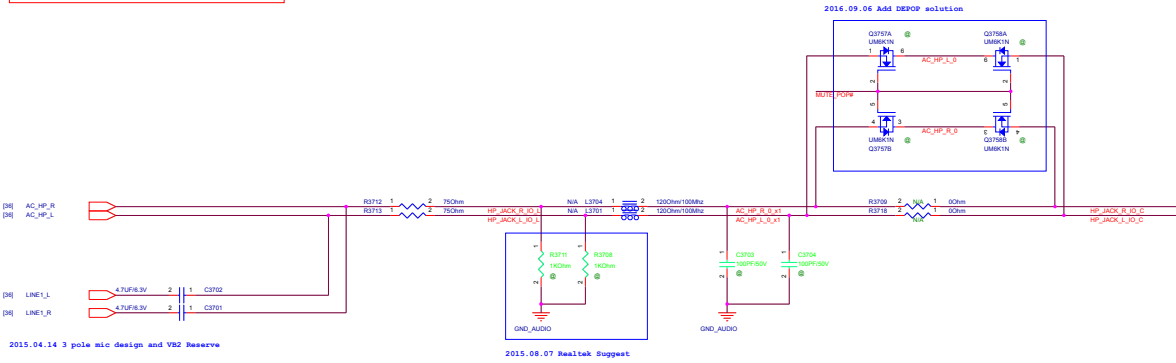
Figure 4. Power sequence

		Project Name	
G711GW			
Title : AUDIO ALCS236-CQVB2			
Store	Dept.:	ASUSTek COMPUTER INC.	Engineer:
Custom			Marshall Li
Date	Tuesday, March 10, 2015	Event	36 of 100

## Headphone&MIC

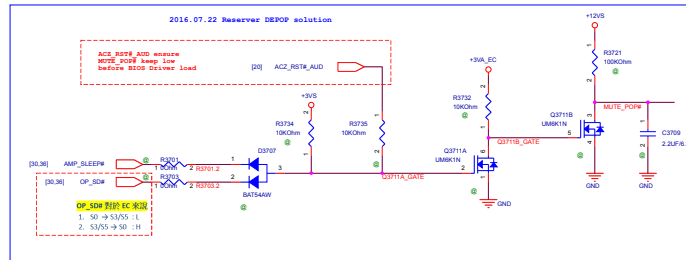


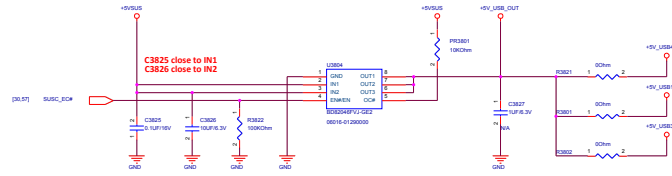
Main Board



## MUTE CONTROL

MUTE CONTROL new solution for 1.8V HDA BUG 0318



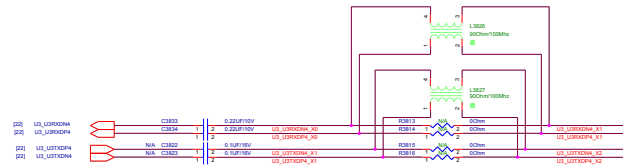


## USB3.0\_PORT4 ( Support USB Charge Circuit )

J3809 USB3.0 Connector  
1st Source: P/N:12013-00015300 FOXCONN/UEA1111-N40AM2-7H  
2nd Source: P/N:12013-00080400 SINGATRON/ZUS4006-310101F

## USB Charge Circuit (For PORT 4)

## USB3.0\_PORT4



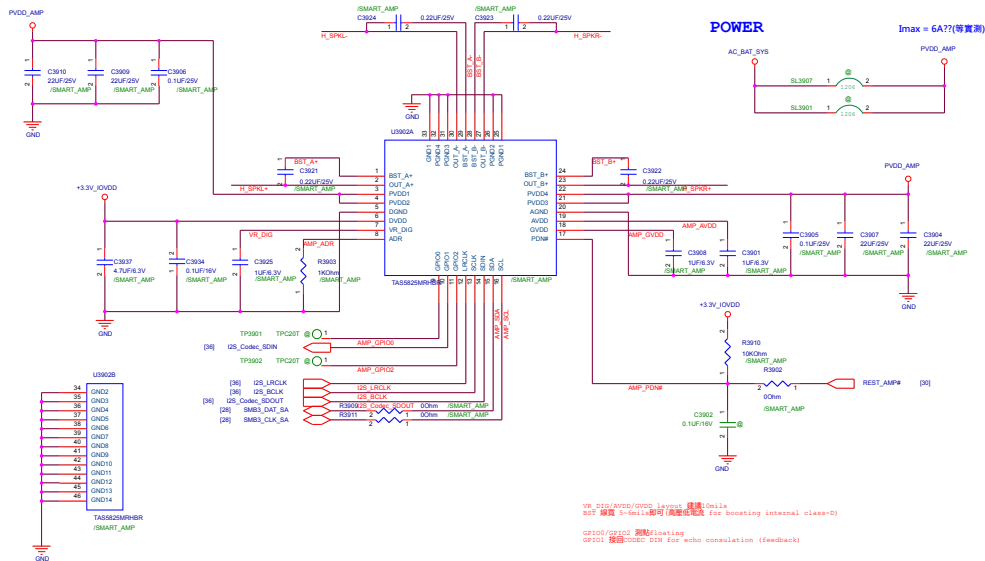
## USB3.0 ESD-Protection



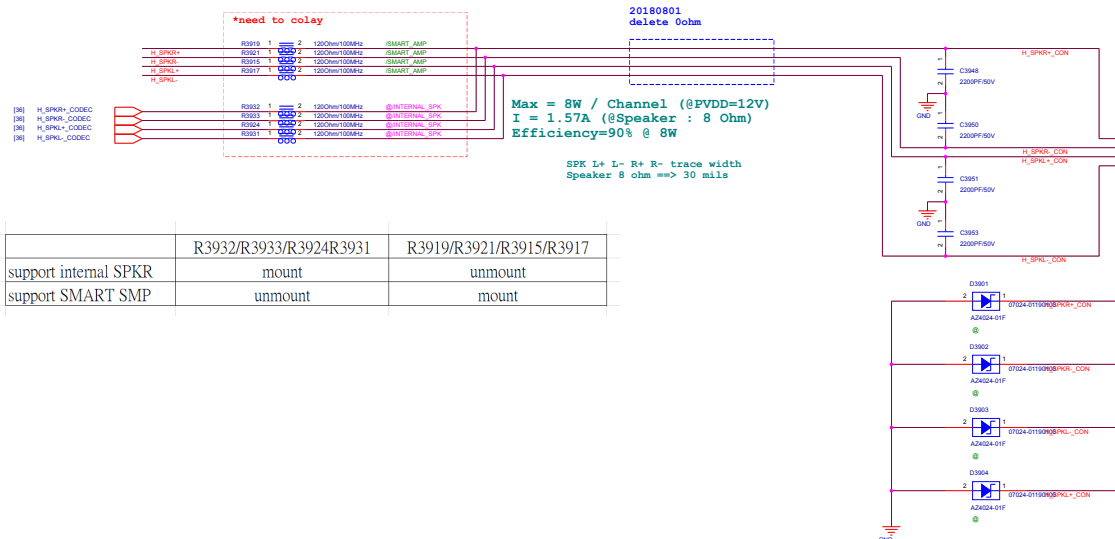
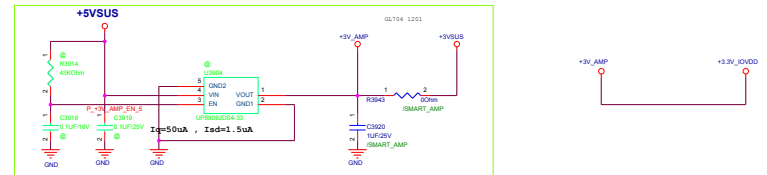
1st : 07G028075030  
ESD PROTECTION AZ1045-04F  
2nd : 07G028153010  
ESD PROTECTION IP4284CZ10-TB

USB3.0 Pin define:	
1 <sup>+</sup>	VBUS <sup>+</sup>
2 <sup>-</sup>	D <sup>-</sup>
3 <sup>+</sup>	D <sup>+</sup>
4 <sup>-</sup>	GND <sup>-</sup>
5 <sup>-</sup>	RX <sup>-</sup>
6 <sup>-</sup>	RX <sup>+</sup>
7 <sup>-</sup>	GND <sup>-</sup>
8 <sup>-</sup>	TX <sup>-</sup>
9 <sup>+</sup>	TX <sup>+</sup>

D3802 ESD Diode  
1st Source: P/N:07024-00200200 AMAZING/AZC009-04SPRTG  
2nd Source: P/N:07024-00710000 NXP/USB2K40

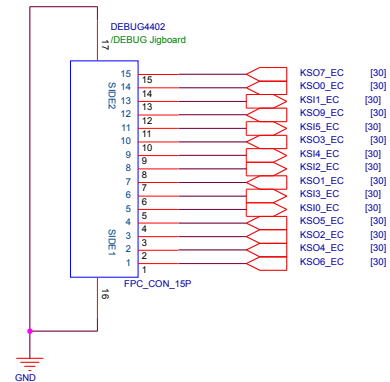
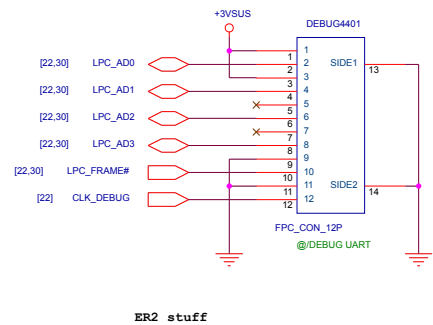


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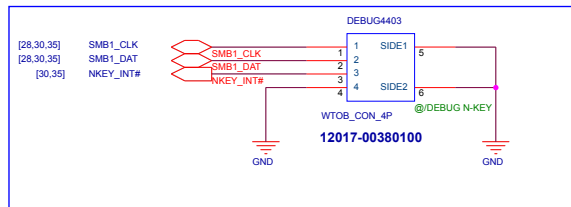





LPC Debug Port

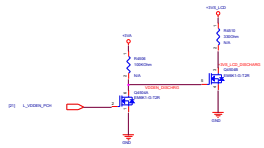


N-KEY Debug Connector

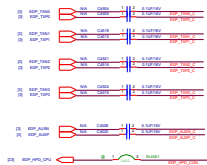


<Variant Name>

		Title : <b>DEBUG_LPC</b>	
ASUSTeK COMPUTER		Engineer: <b>Gaming RD</b>	
Size	Project Name	Rev	
A	<b>G711GW</b>	1.0	
Date: Tuesday, March 19, 2019		Sheet	44 of 103

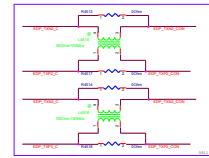
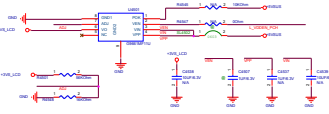


#### eDP from CPU

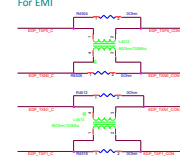


MS10 is selected by panel spec

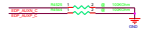
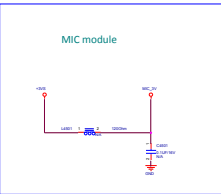
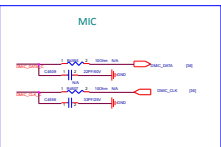
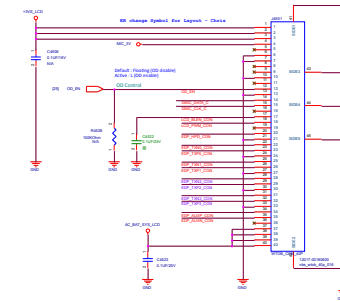
Current Limit vs. $R_{DS(on)}$ Values			
$R_{DS(on)}$ (mΩ)	1000	1500	2000
0.08	2100	1400	1200
0.09	2000	1300	1100
0.10	1900	1200	1000
0.11	1800	1100	900
0.12	1700	1000	800
0.13	1600	900	700
0.14	1500	800	600
0.15	1400	700	500
0.16	1300	600	400
0.17	1200	500	300
0.18	1100	400	200
0.19	1000	300	100
0.20	900	200	0



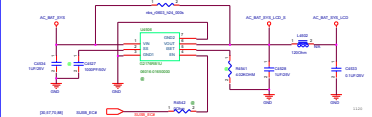
#### For EMI



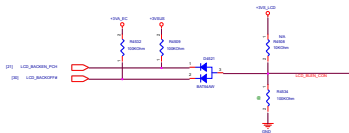
#### eDP Panel Conn.



#### Panel BL Power



#### Panel



# Main Board

20180716a  
Ian: change PD controller to ITE8851  
20180702  
Ian: modify component location



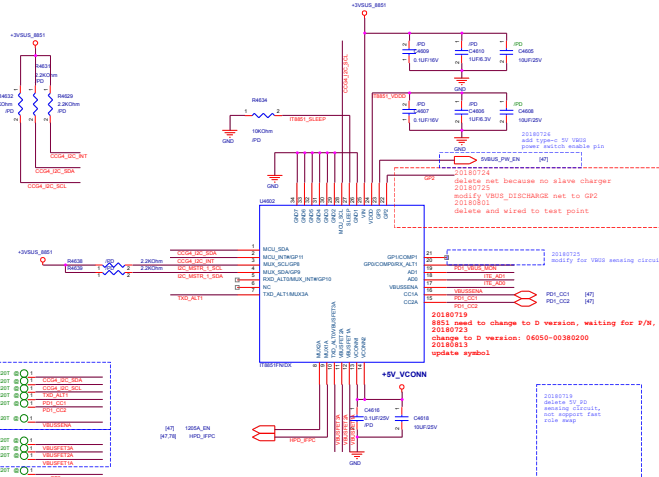
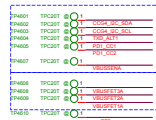
I<sub>max</sub> = 650mA



change to shorted  
and reserve pins  
for head

20180725  
add test point for USB

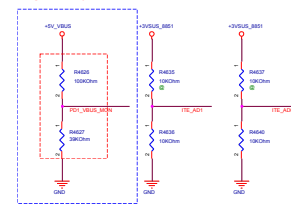
20180725  
add test point for USB



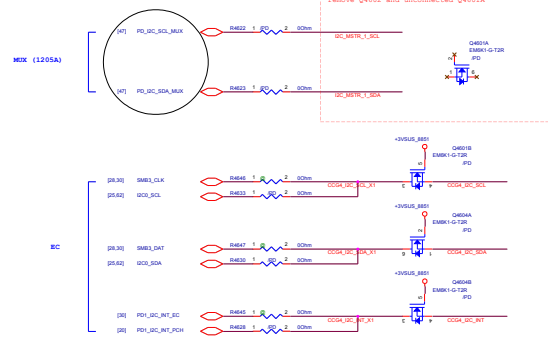
20180719  
B851 need to change to D version, waiting for P/W, part, symbol  
20180723  
change to D version: 06050-00380200  
20180813  
update symbol

20180808  
modify R4624/R4627 resistor

20180801  
modify VBUS sensing circuit



## Different power plan prevent leakage



## 6.3 I2C0 Slave ID Decode

IT8851 provides one I2C slave interface, I2C0, for communication and four different slave ID decodes for I2C0 slave.

Table 6-1. I2C0 Slave ID Decode

AD1	AD0	Slave ID
0	0	7h40
0	1	7h42
1	0	7h50
1	1	7h52

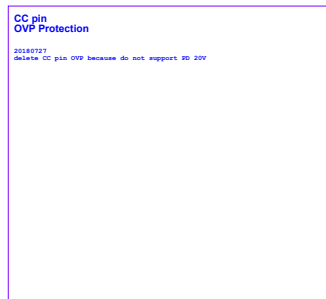
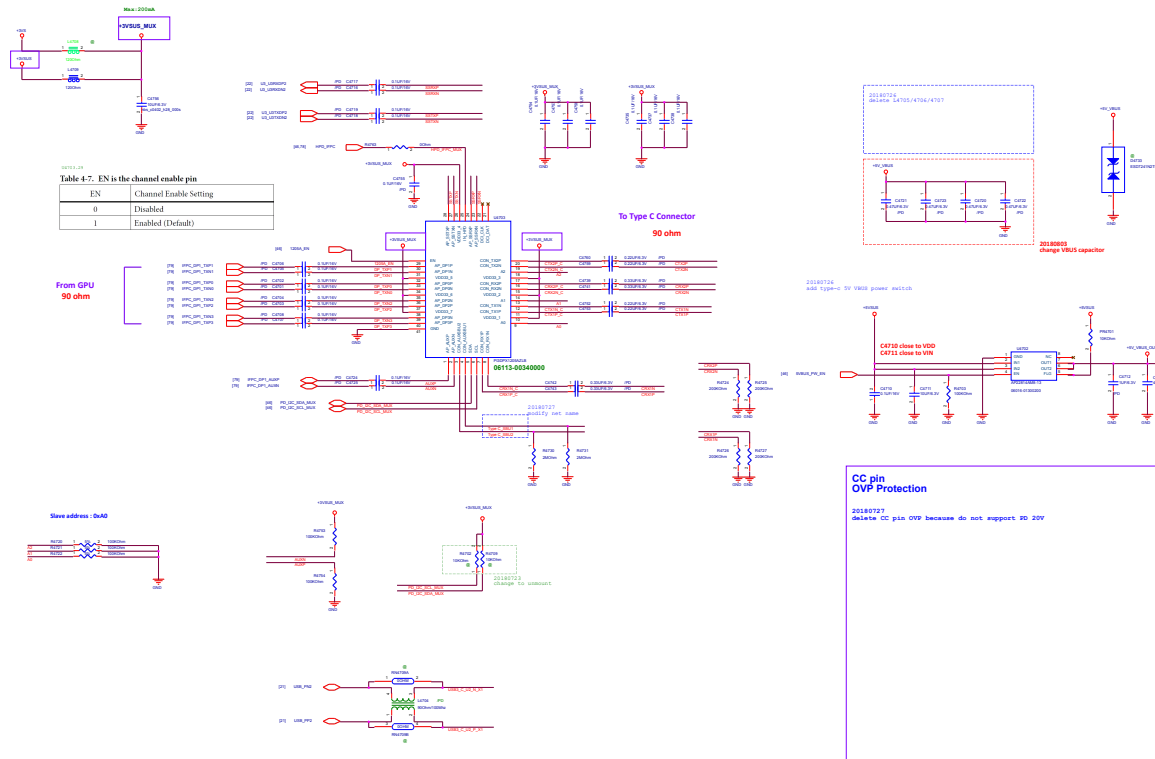


# TYPE-C USB3.1

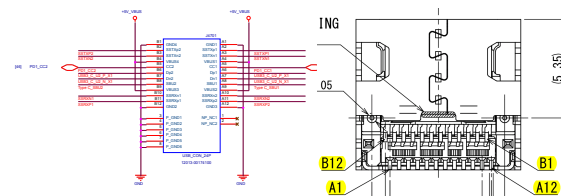
NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V <sub>BUS</sub>	CC1	D+	D-	SBU1	V <sub>BUS</sub>	RX2-	RX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
	GND	RX1+	RX1-	V <sub>BUS</sub>	SBU2	D+	D-	CC2	V <sub>BUS</sub>	TX2-	TX2+	GND

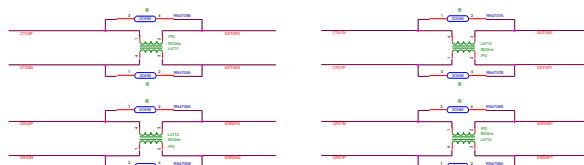
NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.



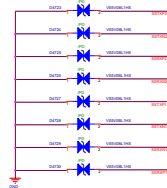
## TYPE-C Connector



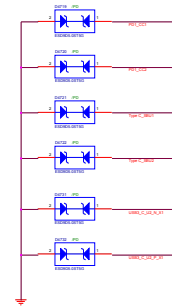
## USB EMI-Protection



## USB3.0 ESD-Protection



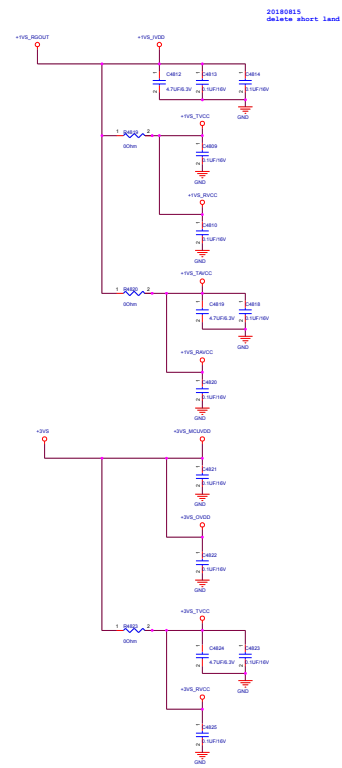
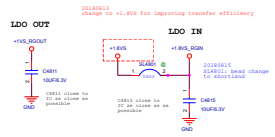
## USB2.0 ESD-Protection



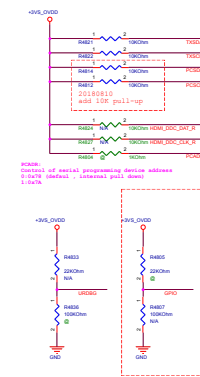
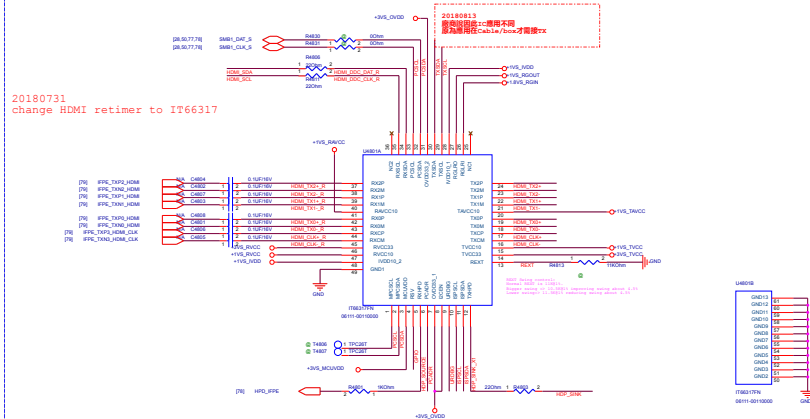
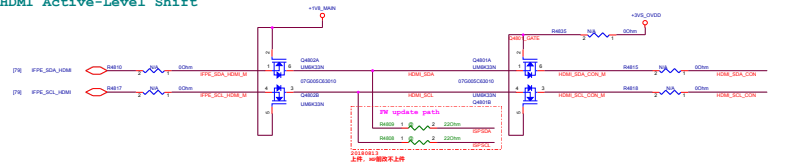
## PD Discharging

20180901 no PD function, delete discharging circuit

# Internal Regulator option



# HDMI Active-Level Shift



Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

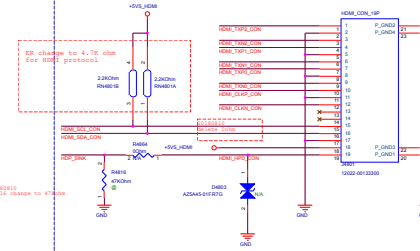
20180807  
add for output swing SW control

# Main Board

## HDMI PWR\_+5VS\_HDMI

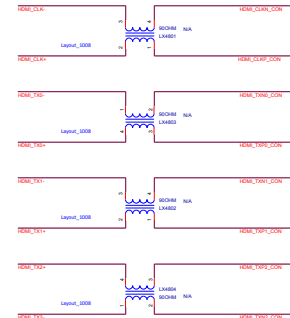


## HDMI Conn.



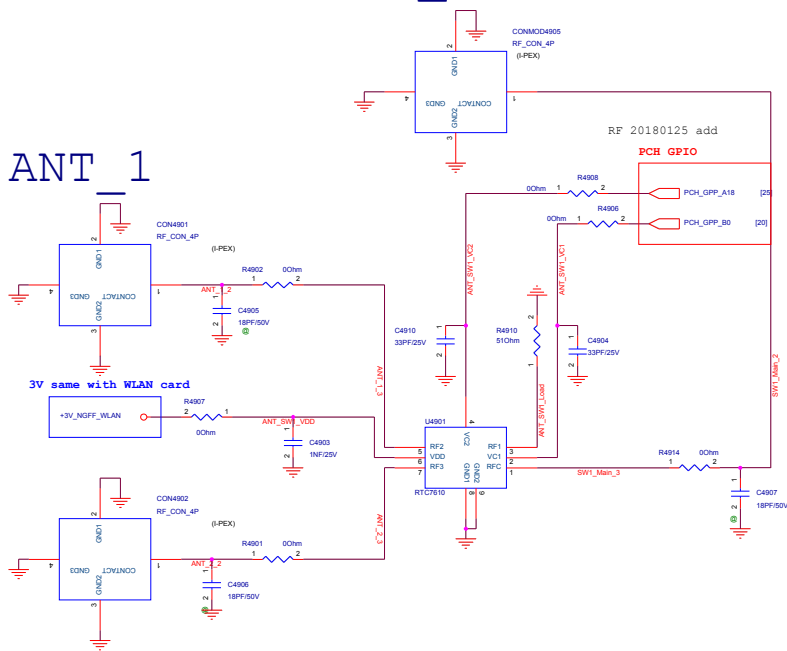
## HDMI EMI

## teknisi indonesia



Project Name		Rev
ASUS G711GW		1.1
Title : HDMI		
Des	Dept.:	Engineer: EE1_R03
Drawn	Checked	By

Module\_AUX



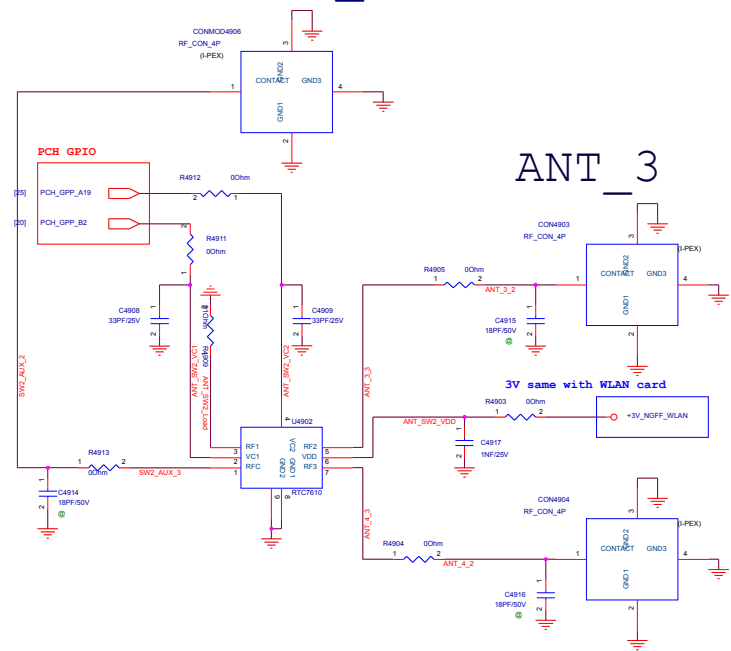
ANT\_1

ANT\_2

U4901 RTCT7610				
ANT	Port	VC1 GPP_B0	VC2 GPP_A18	
50 Ω	RF1	1	0	
ANT_1	RF2	X	1	
ANT_2	RF3	0	0	

X: don't care  
0: -0.2v~0.3v  
1: 1.6v~3.6v

Module\_MAIN



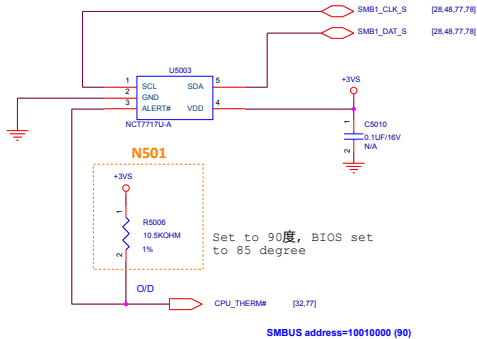
ANT\_3

ANT\_4

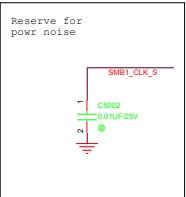
U4902 RTCT7610				
ANT	Port	VC1 GPP_B2	VC2 GPP_A19	
50 Ω	RF1	1	0	
ANT_3	RF2	X	1	
ANT_4	RF3	0	0	

X: don't care  
0: -0.2v~0.3v  
1: 1.6v~3.6v

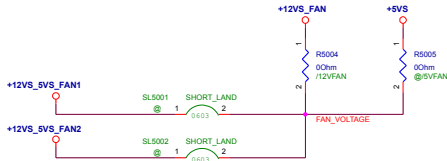
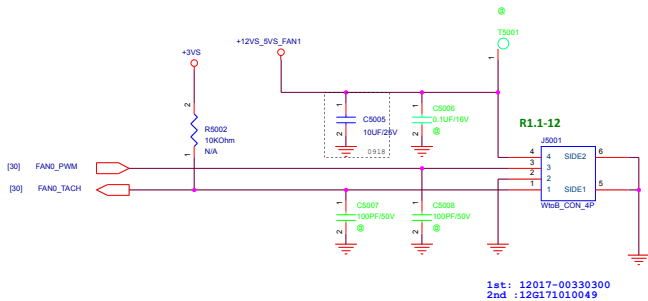
# CPU Thermal Sensor



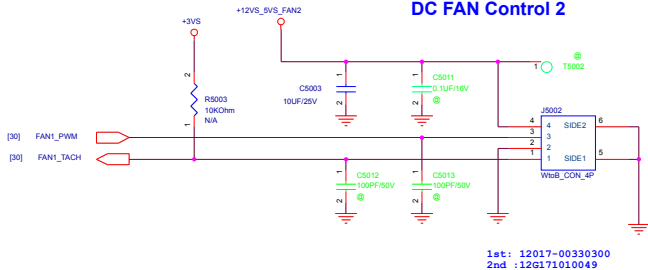
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

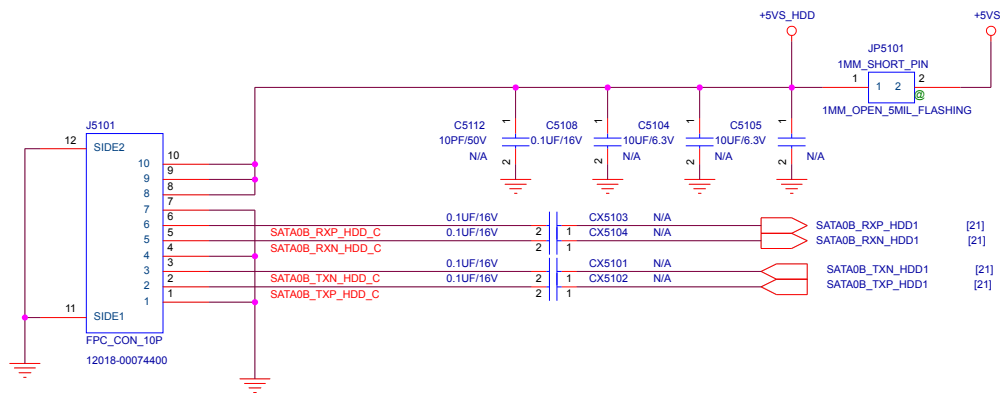


# DC FAN Control 1

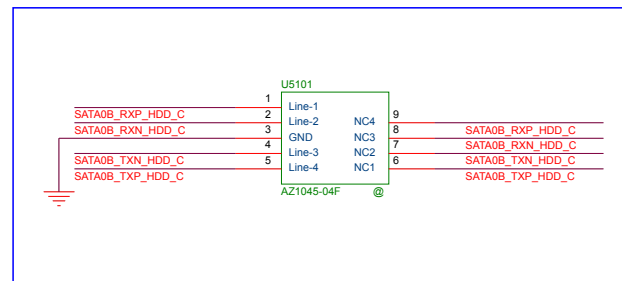


# DC FAN Control 2




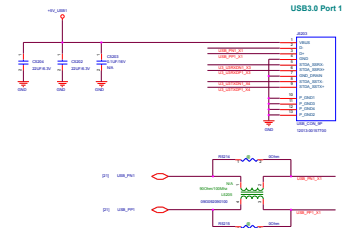


PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND



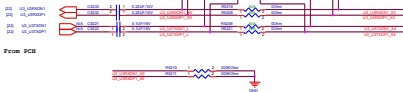
<Variant Name>

		<b>Title :</b> XDD_HDD & ODD CON
ASUSTek COMPUTER		<b>Engineer:</b> Gaming RD
Size A	Project Name G711GW	Rev R1.0
Date: Tuesday, March 19, 2019		Sheet 51 of 103

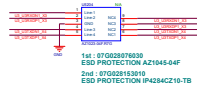


### USB3\_0 EMI-Protection

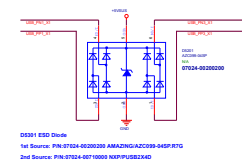
1370025  
1370025  
1370025



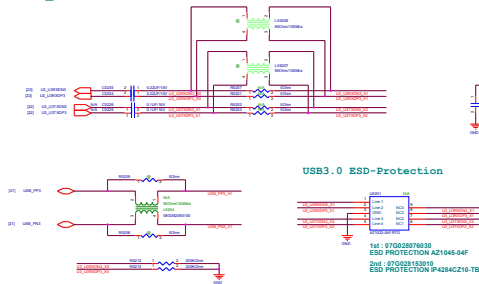
### USB3.0 ESD-Protection



### USB2.0 ESD-Protection



### USB3.0\_PORT3

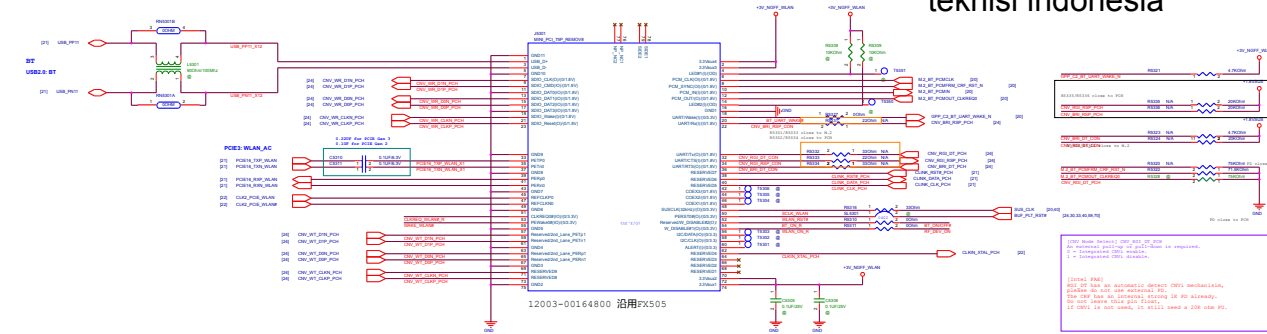


R11-02

## NGFF M.2 TYPE\_E-KEY WIFI

Main Board

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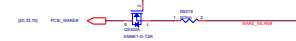


J5361\_NGFF E-KEY WLAN Connector H=2.8mm  
1st Source: P/N:12003-00076900 ARGOSY/NAS80-S4761-TP20  
2nd Source: P/N:12003-00076900 ARGOSY/NAS80-S4761-TP20  
3rd Source: P/N:12003-00076900 LOTES/AP0802-P814

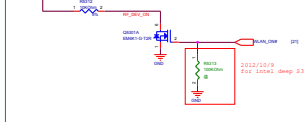
### WLAN CLKREQ#



### WLAN\_Wake# Control



### WLAN & BT ON



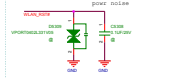
To watch WIGL test flow to  
BT wake up to signal watch  
1.0s (if use case to +3V, let  
BT use wake quickly when  
BT wake up)

High active

80S PWR

Project which use the control schematic should  
make sure that BT ON signal can't be High at  
0.5V/1.0V when BT power is on

### For EMI

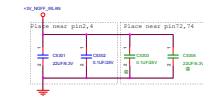
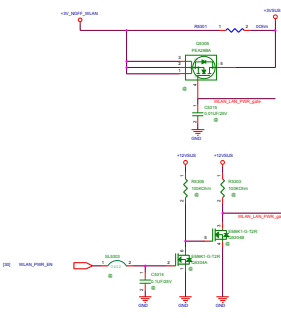


### NFC CONTROL PART

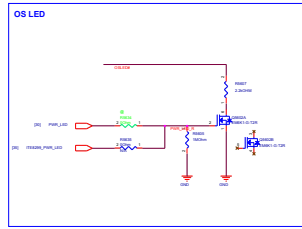


### WLAN PWR\_+3V\_NGFF\_WLAN (Non-ICST)

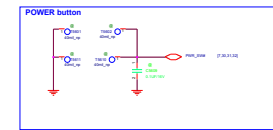
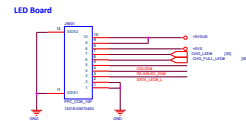
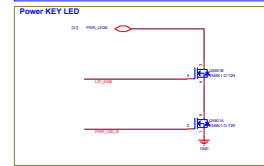
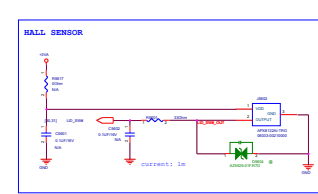
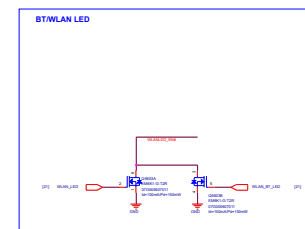
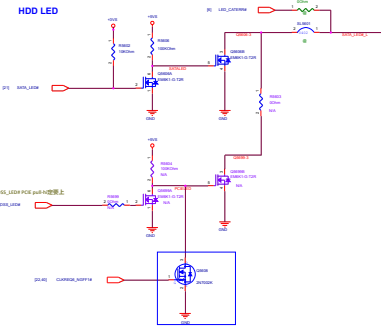
Support ASUS Open Cloud Computing (ASOC) mode  
WLAN PWR to +3V305



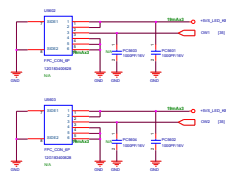
Title : WFIWMax	
Author : WFIWMax	Engineer : EE
Rev : 1.0	Rev : 1.0
QX5020X	
Rev : 1.0	



2014/05/29 Add HDD & SSD LED control circuit.



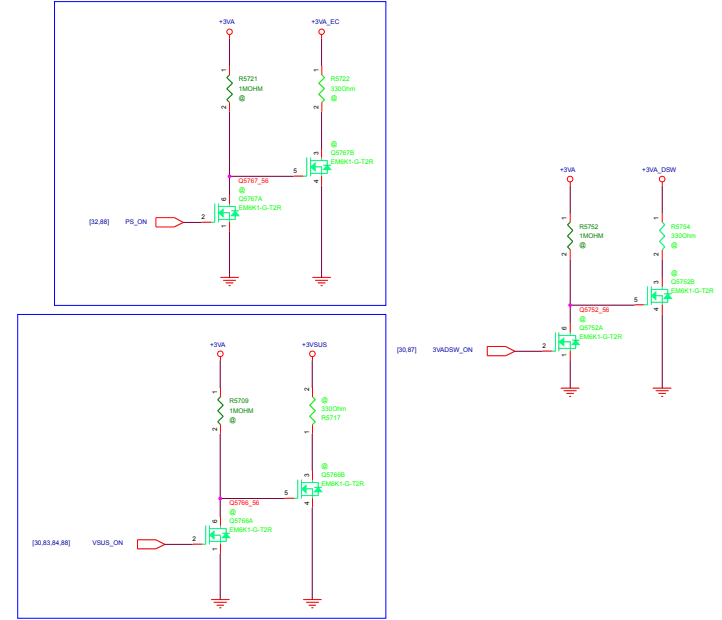
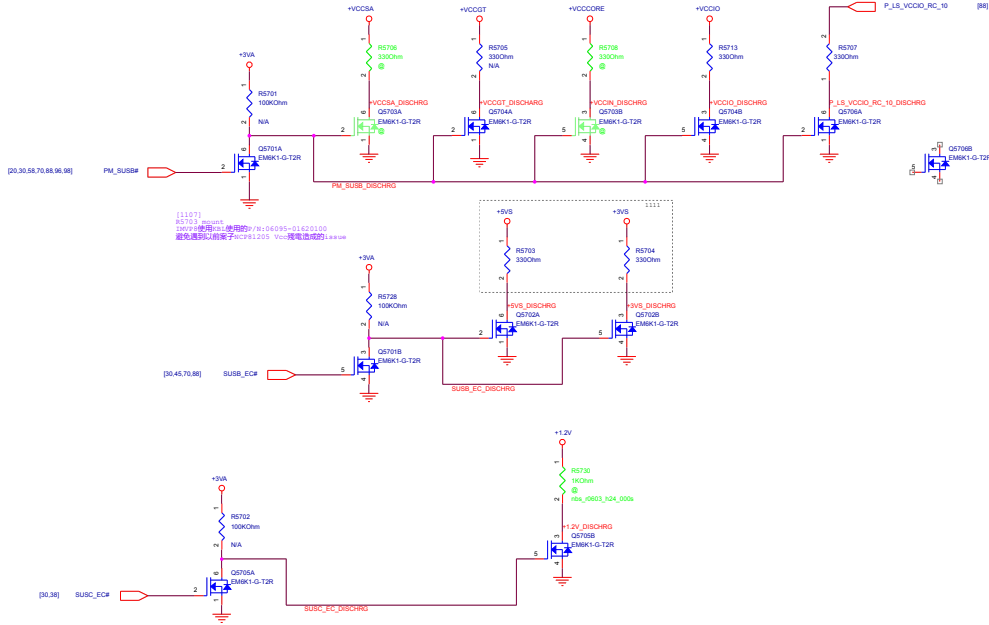
One-wire Connect to LED



Title : LED & I/O	
Designer : Gaining HD	
Rev : 01	Q7110W
Rev : 01	Rev : 01

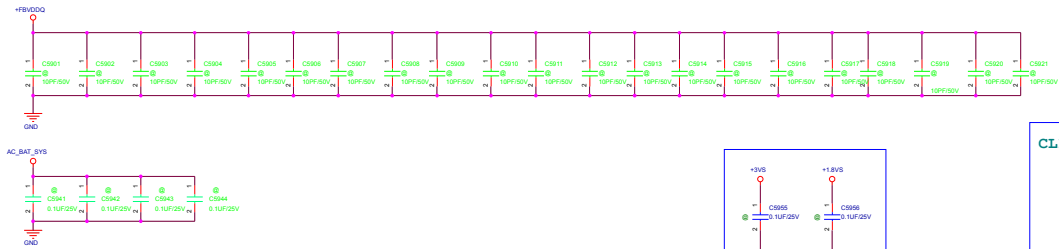


R0.1-02 R0.1-27 R1.0-17

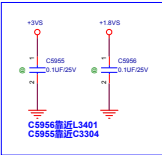
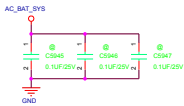




EMI

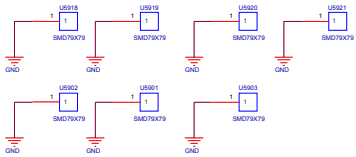


EMI

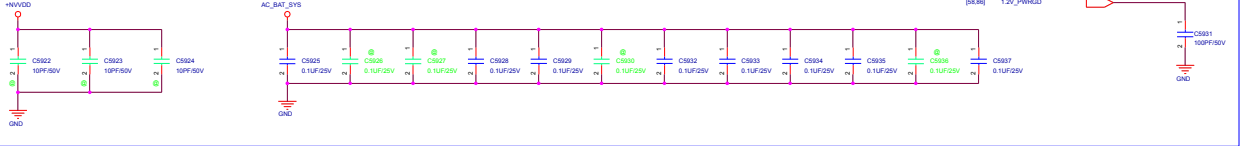


CLIP

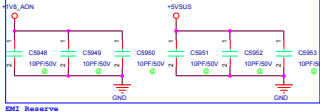
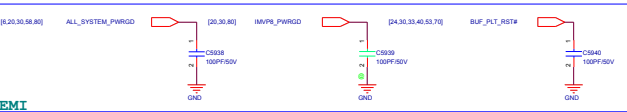
13NB0I40T01011



EMI



EMI

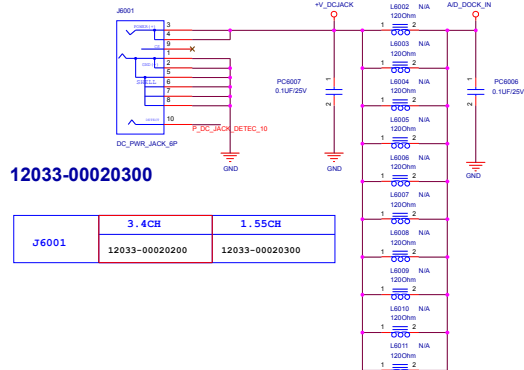


ASUS		Title : I/O Main board Com.	
ASUS MAX COMPUTER		Engineer: Gaming RD	
Size	Project Name	Rev	
C	G711GW	1.0	
Date: Tuesday, March 16, 2010		Sheet	58 of 100

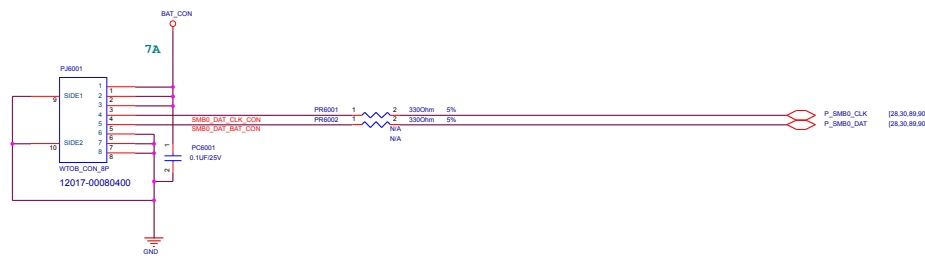
## DC-IN Connector

DC Jack使用請詢用River\_Hsu

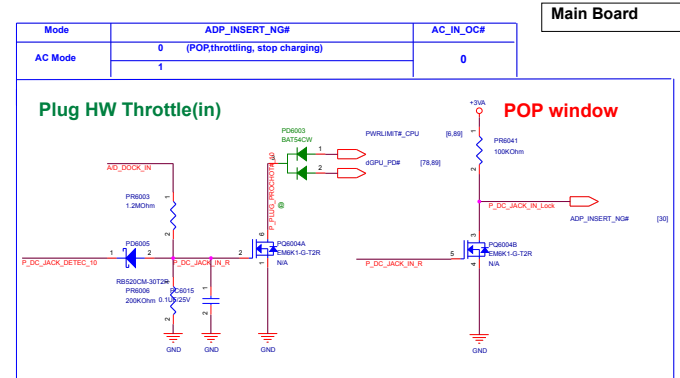
New 6 Phi 4 Pin DC\_Jack




## Battery Connector

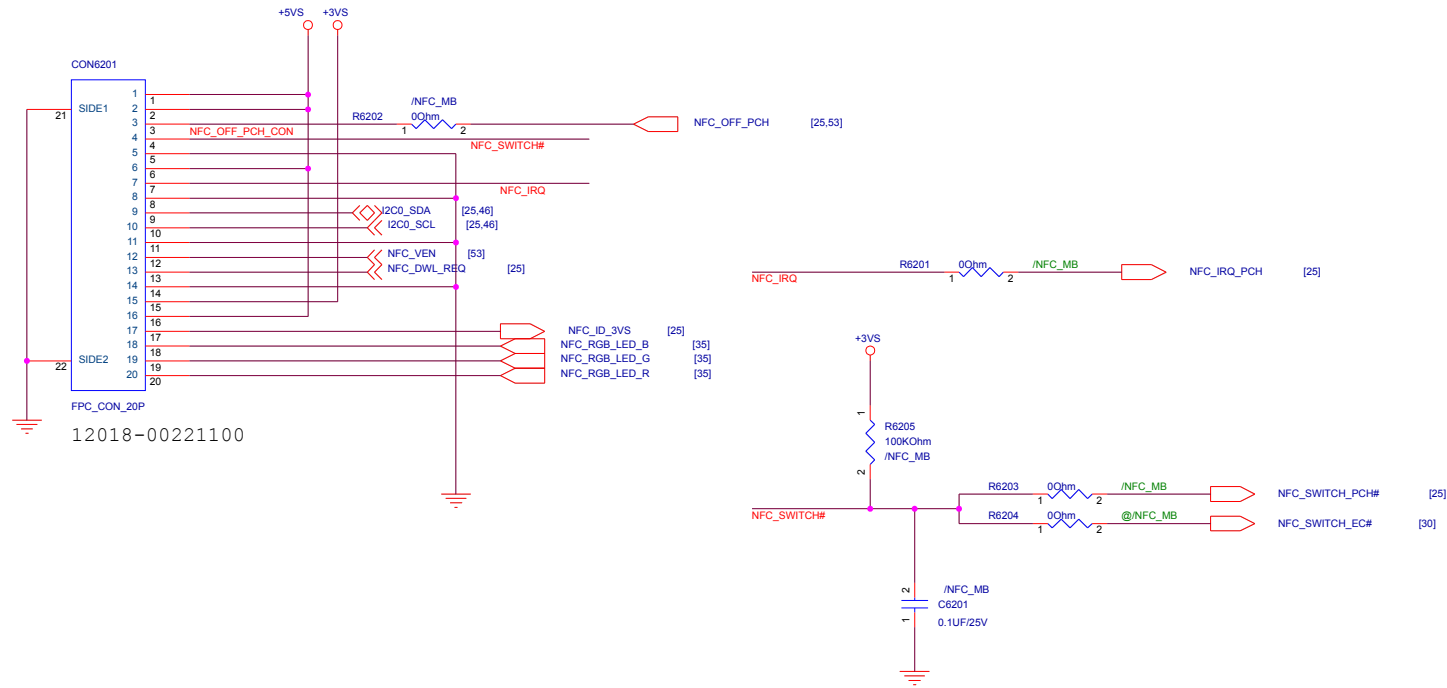


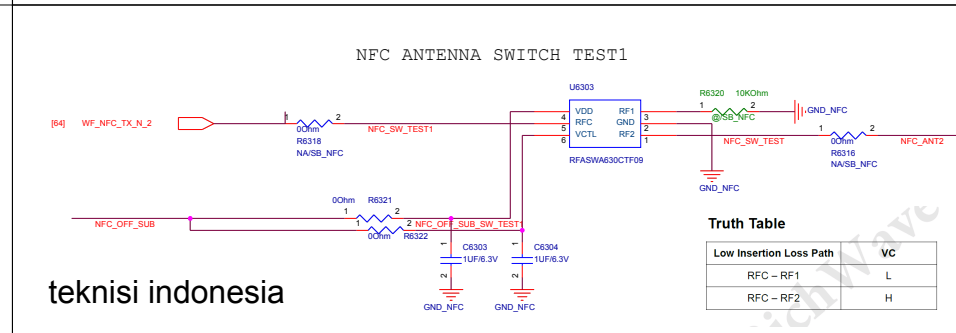
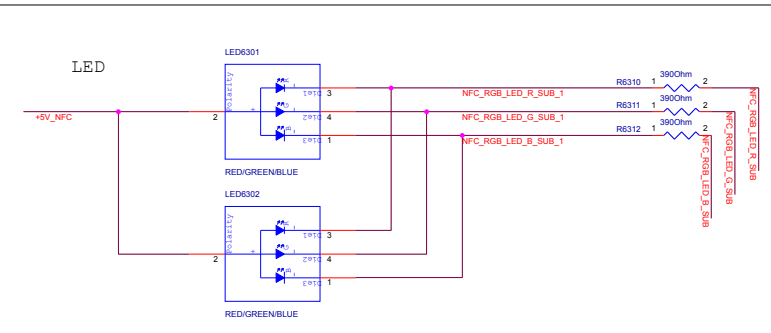
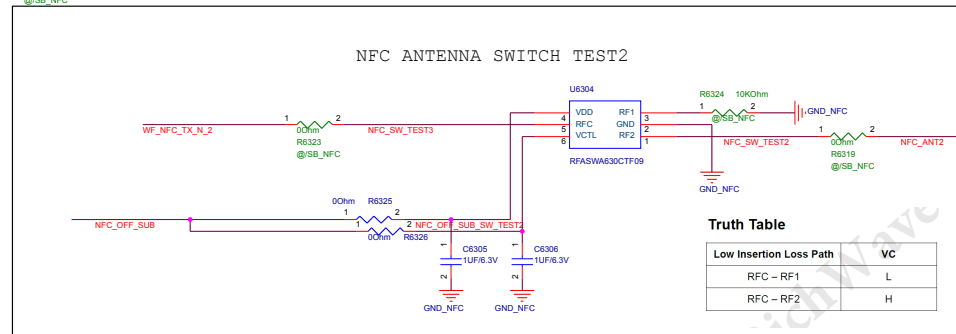
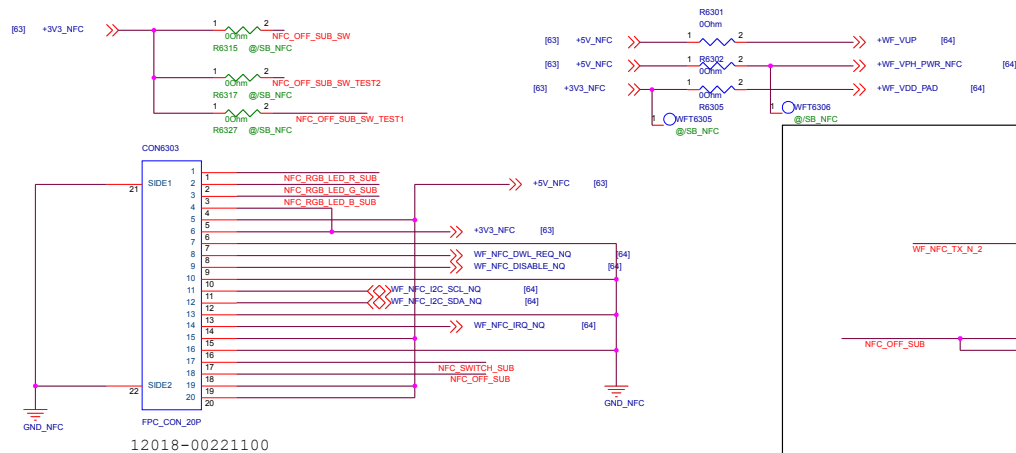
Note: Battery Connector 正確性與BAT1\_IN\_OC#是否預留!



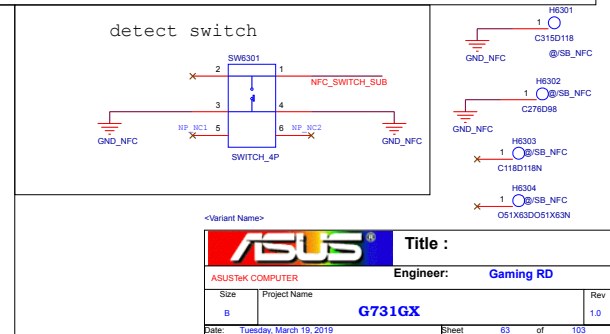
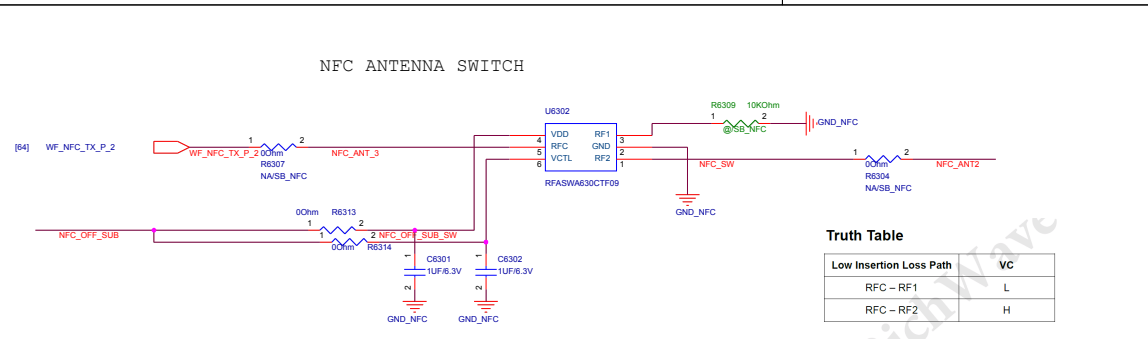
		Project Name <b>GX700</b>		Rev <b>R1.0</b>
<b>Title :</b> <b>DC &amp; BAT IN</b>				
Size <b>A3</b>	Dept.: <b>NB_Power team</b>		Engineer: <b>Benson</b>	
Date: <b>Tuesday, March 19, 2019</b>			Sheet <b>60</b> of <b>103</b>	

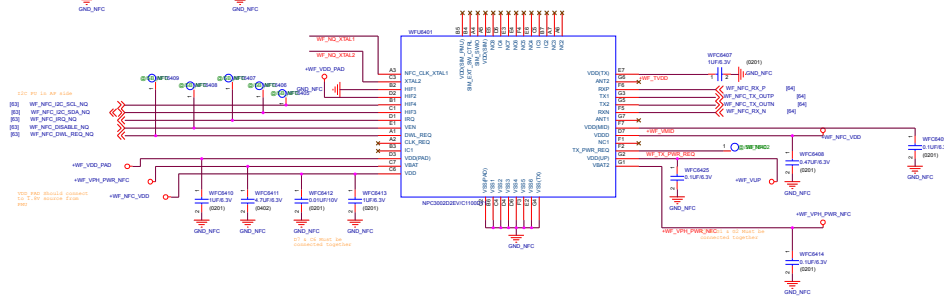




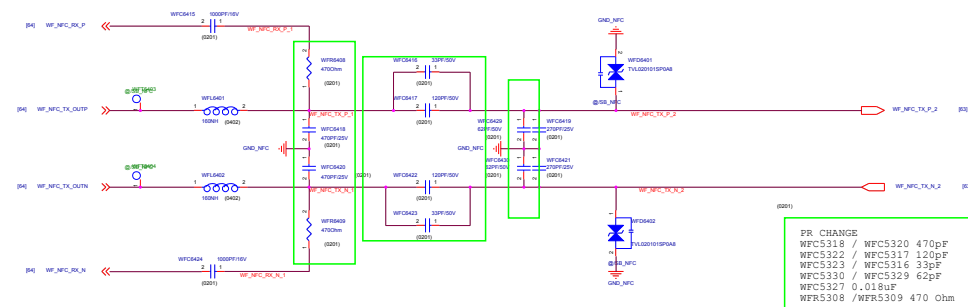


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## NFC Matching



ASUS		Title : USB_****	
ASUSTek COMPUTER		Engineer: Gaming RD	
Size C	Project Name G731GX		Rev 1.0
Date Sunday, March 19, 2017	Printed	64	of 103



Technical drawing of a mechanical part, likely a manifold or housing, showing multiple views (top, side, and detail) with dimensions and labels. The drawing includes various holes, slots, and features labeled with dimensions like Ø3.7, Ø6.5, Ø8, and Ø2.5. It also shows internal features like H-0, H-1, H-2, H-18, and H-15, and a detail view of a corner with R1.5 and R0.75 fillets.

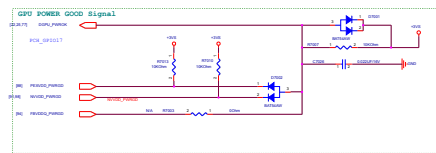
Figure 1: Schematic diagram of the test rig. The diagram shows a mechanical assembly with various components labeled with dimensions and part numbers. Key components include a motor (M1), a pump (P1), a valve (V1), and a pressure sensor (PS1). Dimensions are given in millimeters (mm). A table on the right lists the components and their specifications.

Component	Specification
M1	Motor
P1	Pump
V1	Valve
PS1	Pressure sensor

Technical drawing of a mechanical part. The main view shows a cross-section of a part with a central hole. The hole has a diameter of  $\varnothing 8$  and a depth of  $H=0$ . The part has a base diameter of  $\varnothing 4.2$ . A detail view of the hole is shown to the right, indicating a diameter of  $\varnothing 8$  and a depth of  $H=0$ .

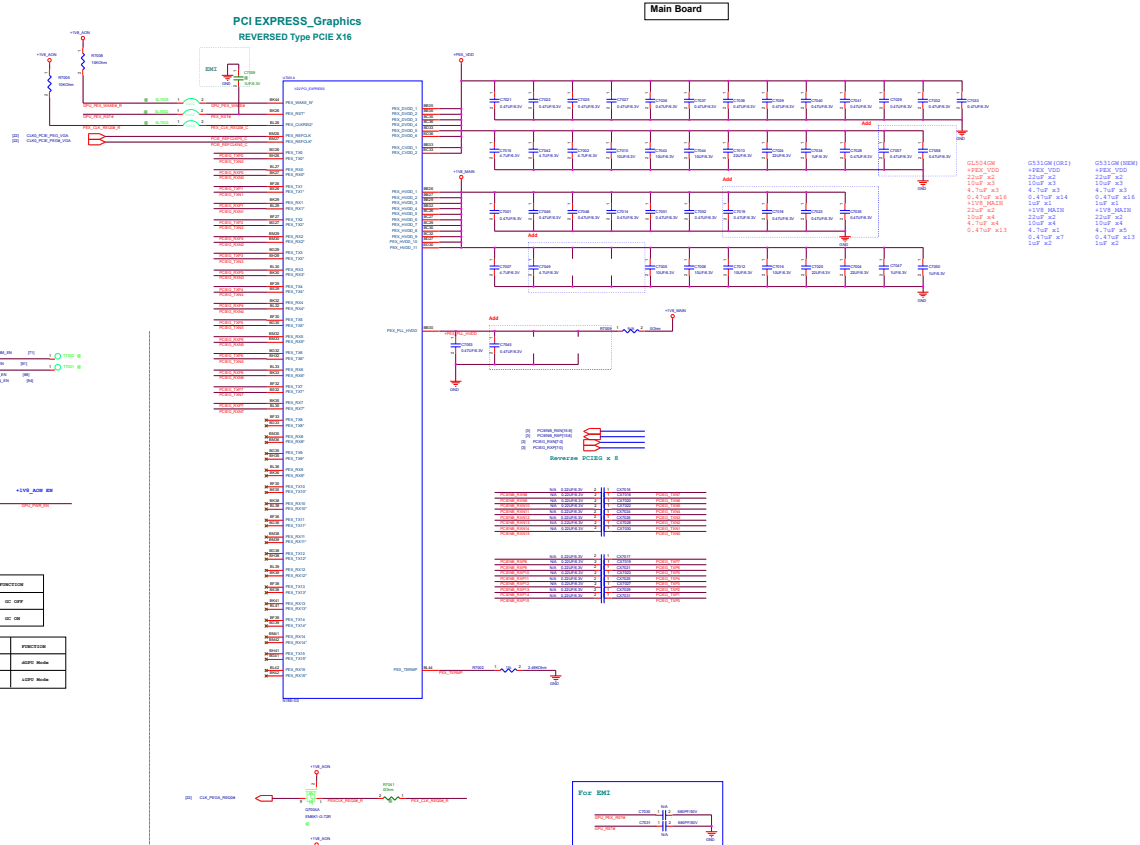
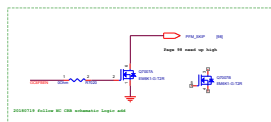
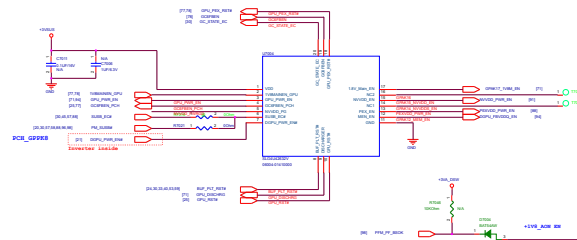
Technical drawing of a mechanical part showing dimensions: R1.5, R1.5, 4, and a coordinate system with origin H0010.

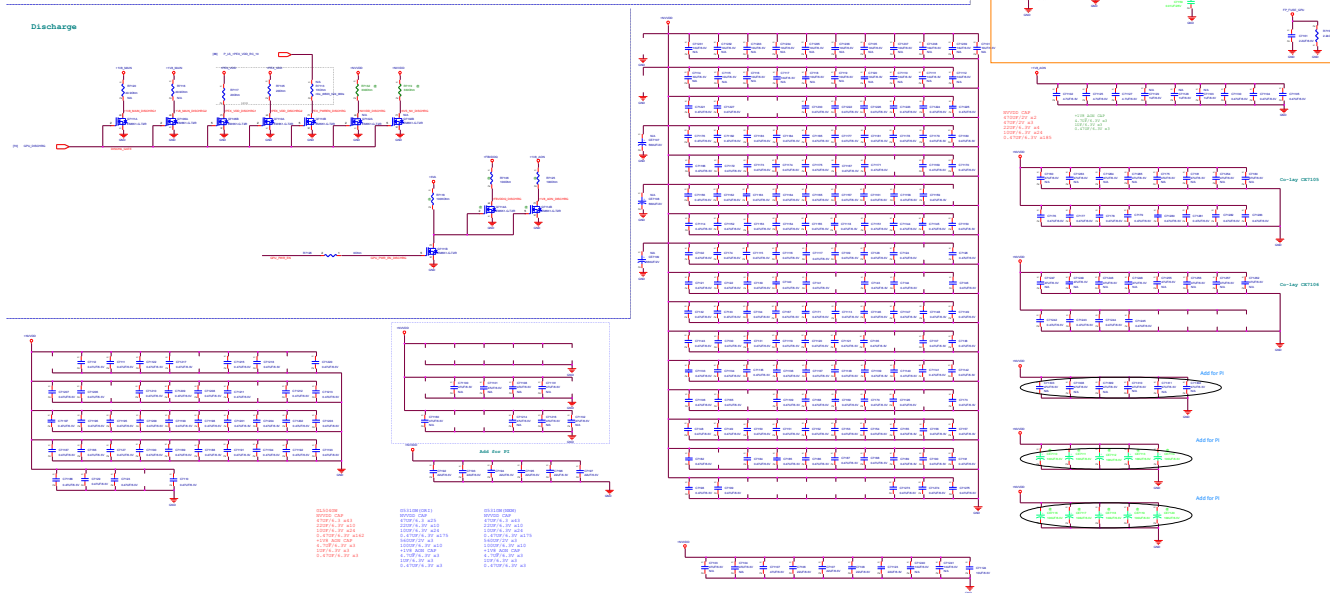
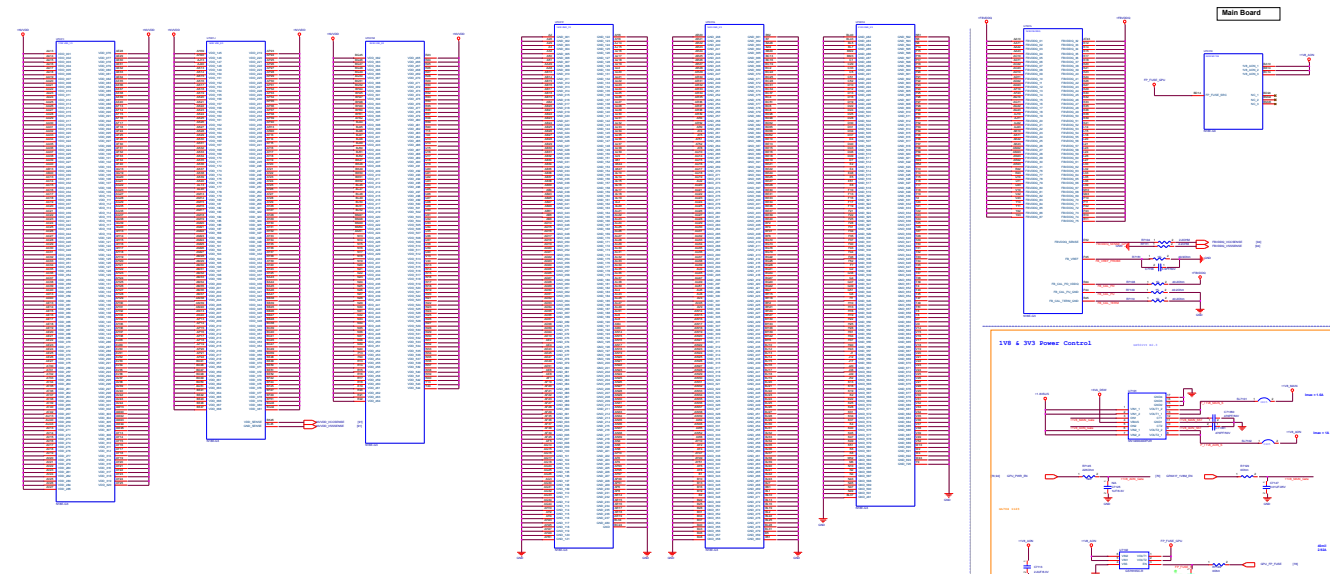
ASUS		Title : ME_Screw Hole & Nut	
ASUSTek COMPUTER		Engineer: Gaming RD	
Size	Project Name		Rev
D	G711GW		1.0



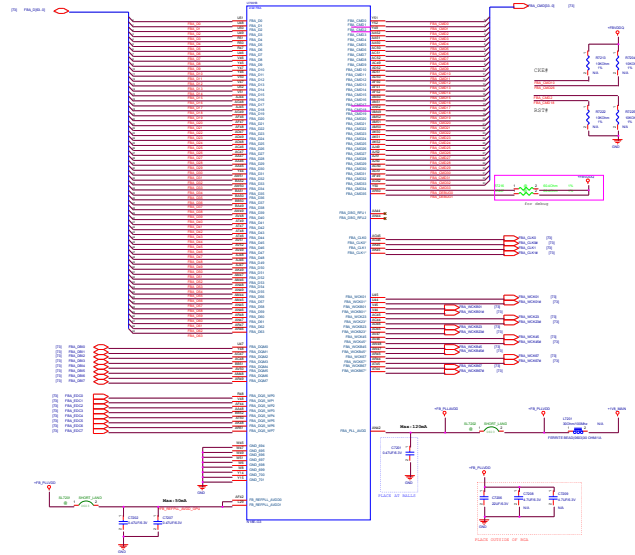
NVVDD POWER GOOD LOOPBACK

## GPU POWER SEQUENCE CONTROL

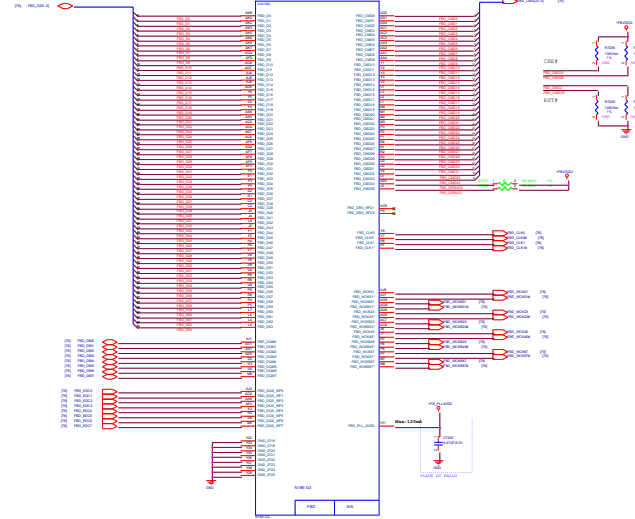




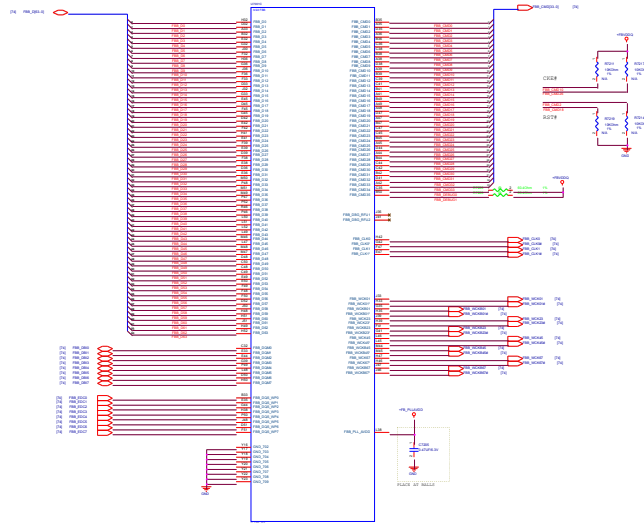
MEMORY: GPU FB Partition A



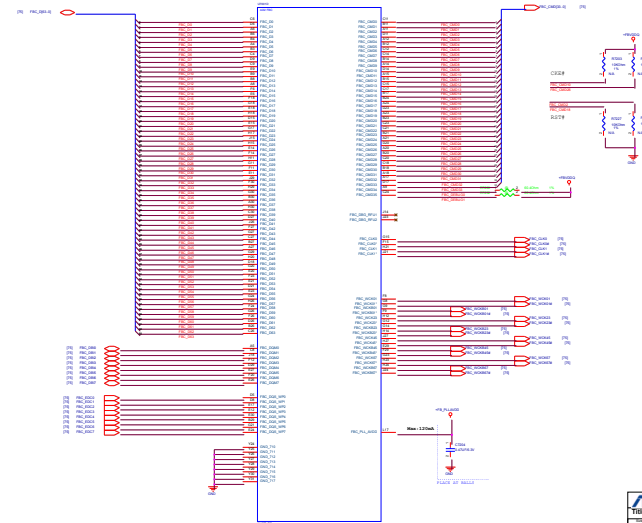
MEMORY: GPU FB Partition D

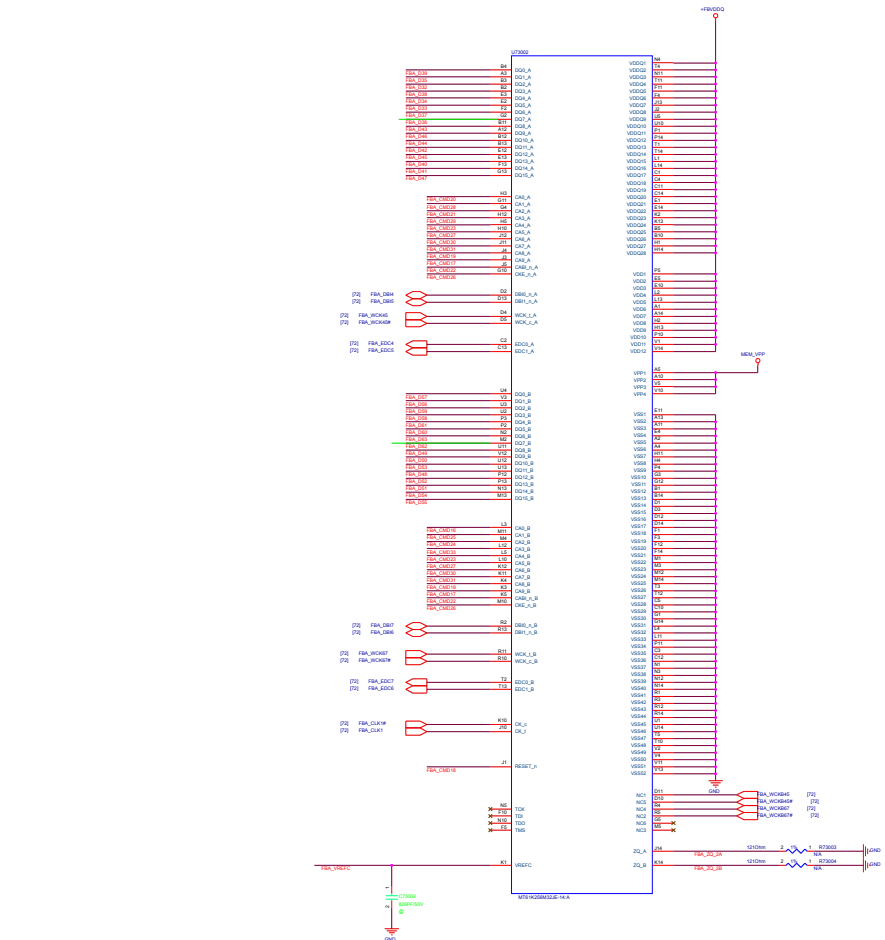
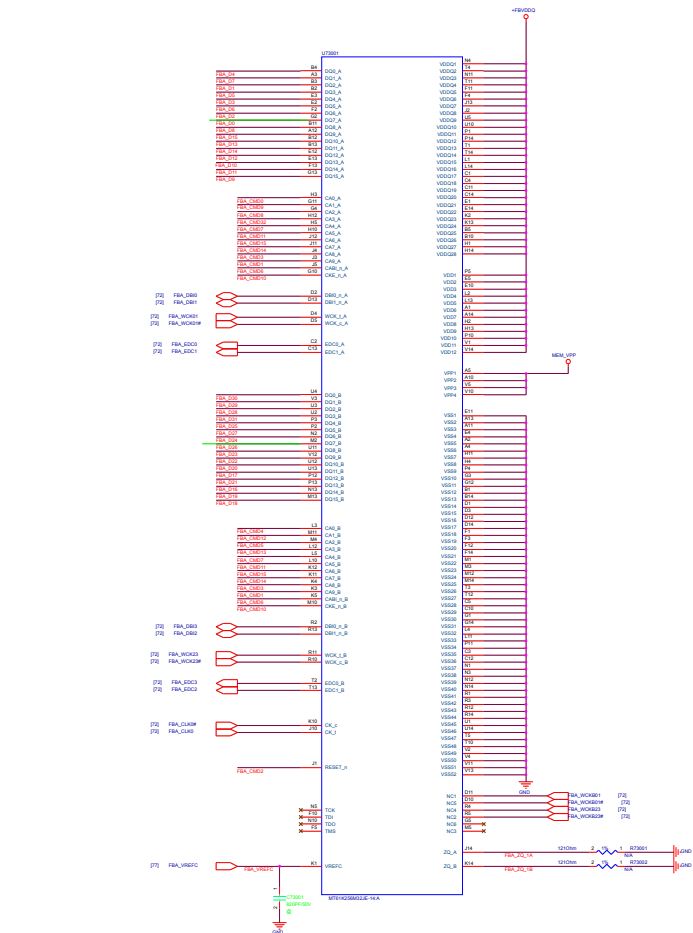


MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C





[72] `FWB_Q[31..0]` 

[72] `FWB_CMC[33..0]` 



(72) F88\_C(83..32) 



853.0

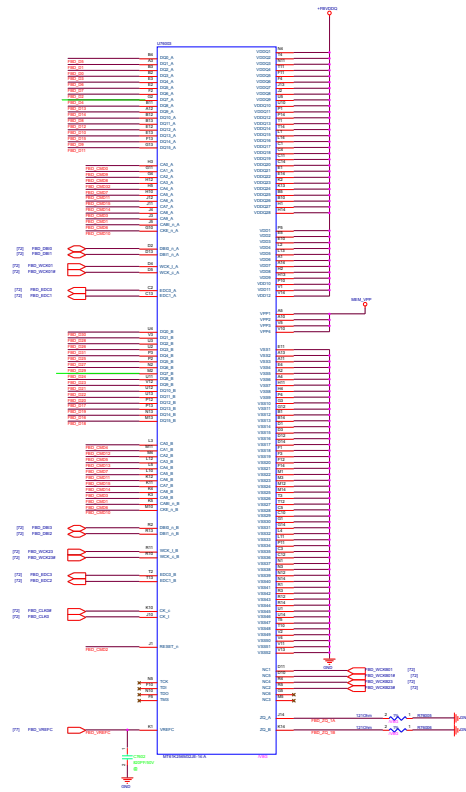
[72] PBC\_Q[31..0] 

[72] PBC\_CMD[33..0] 



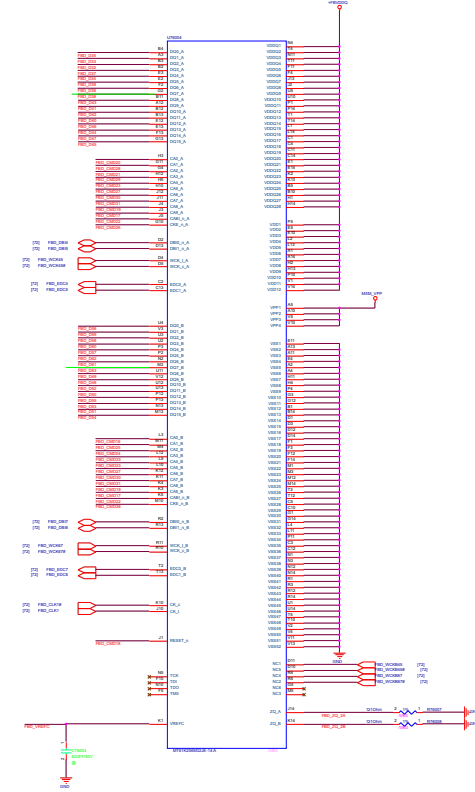
40 Ohm\_NET  
FBD Partition 31..0  
MF=1 Mirror

[70] FBD\_001-0  
[70] FBD\_00000-0



40 Ohm\_NET  
FBDPartition 64..32  
MF=0 Normal

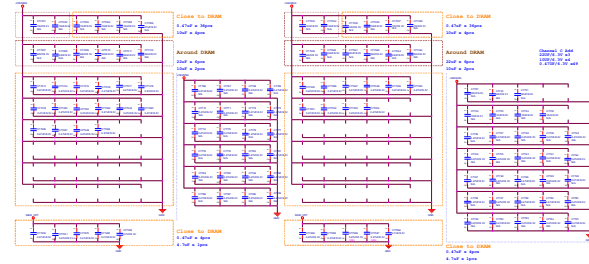
[70] FBD\_001-0



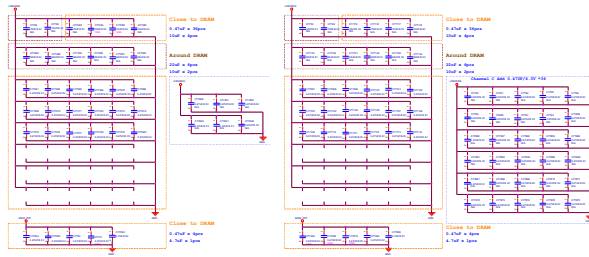
Legend	
Symbol	Description
AND	AND gate
OR	OR gate
NOT	NOT gate
XOR	XOR gate
...	...



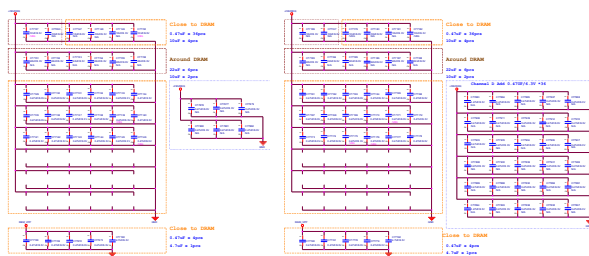
Channel A



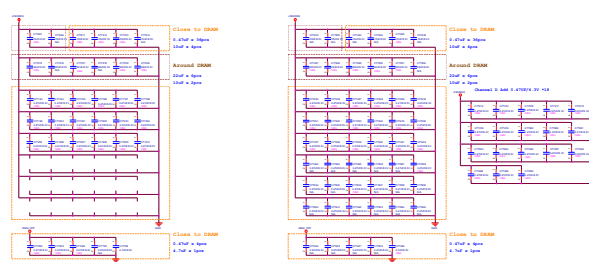
Channel B



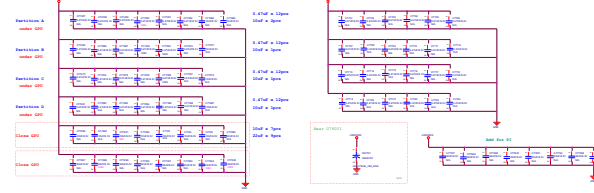
Channel C



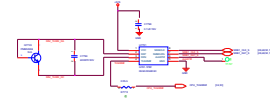
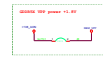
Channel D



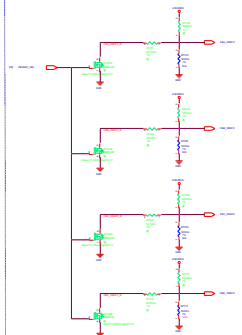
VRAM PWR\_FSVDDQ



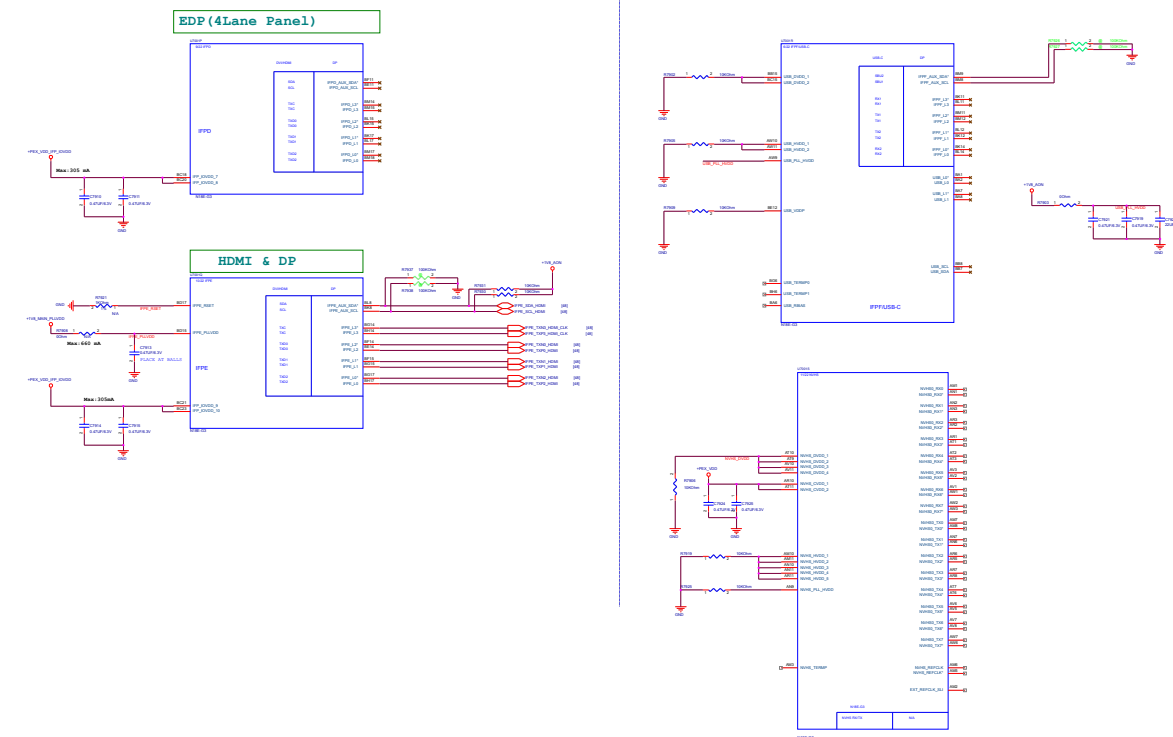
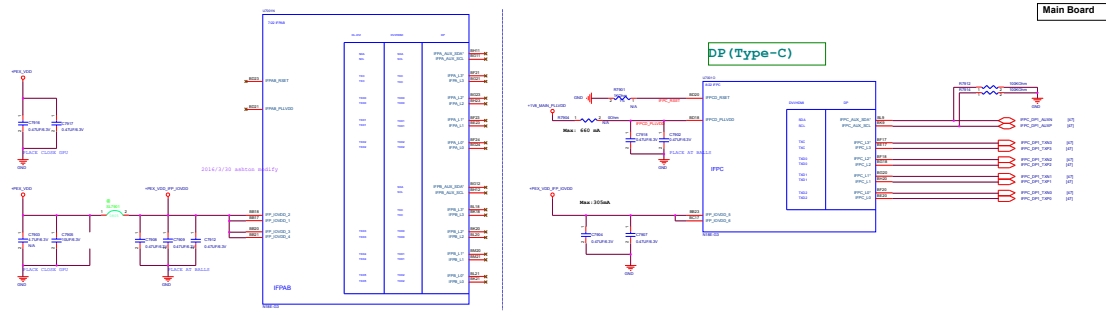
For power sequence measurement



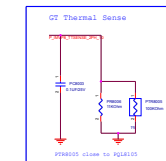
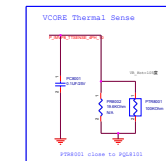
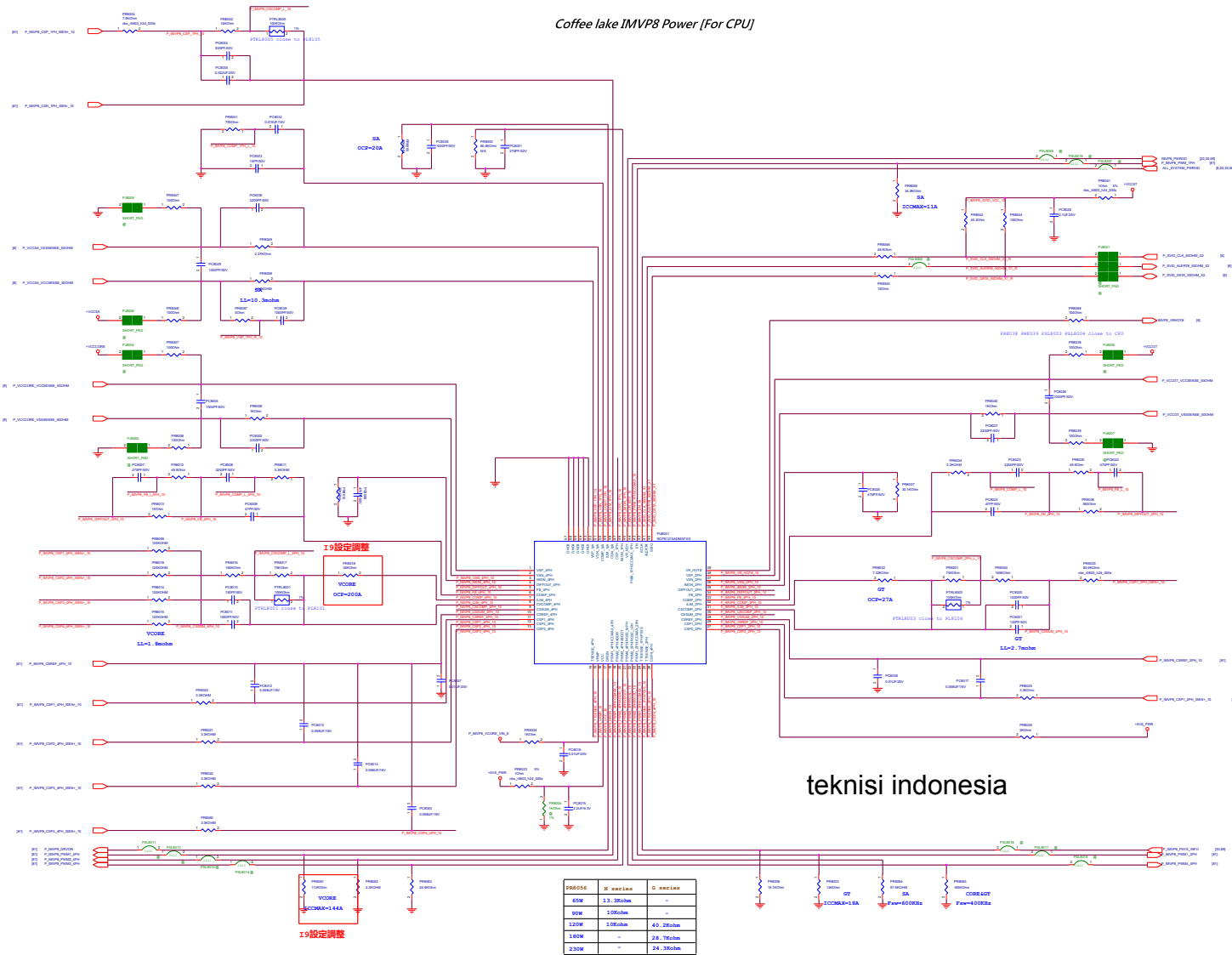
Power sequence measurement results for Channel A, B, C, and D. The results show the power sequence measurement for each channel and the power sequence measurement for the VRAM PWR\_FSVDDQ.







*Coffee lake IMVP8 Power [For CPU]*



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FR056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

 Project Name: <b>GL704GM</b>	
Title: <b>PW_Coffinlake (1)</b>	
Dept.: <b>NB Power team</b>	Engineer: <b>Hon</b>



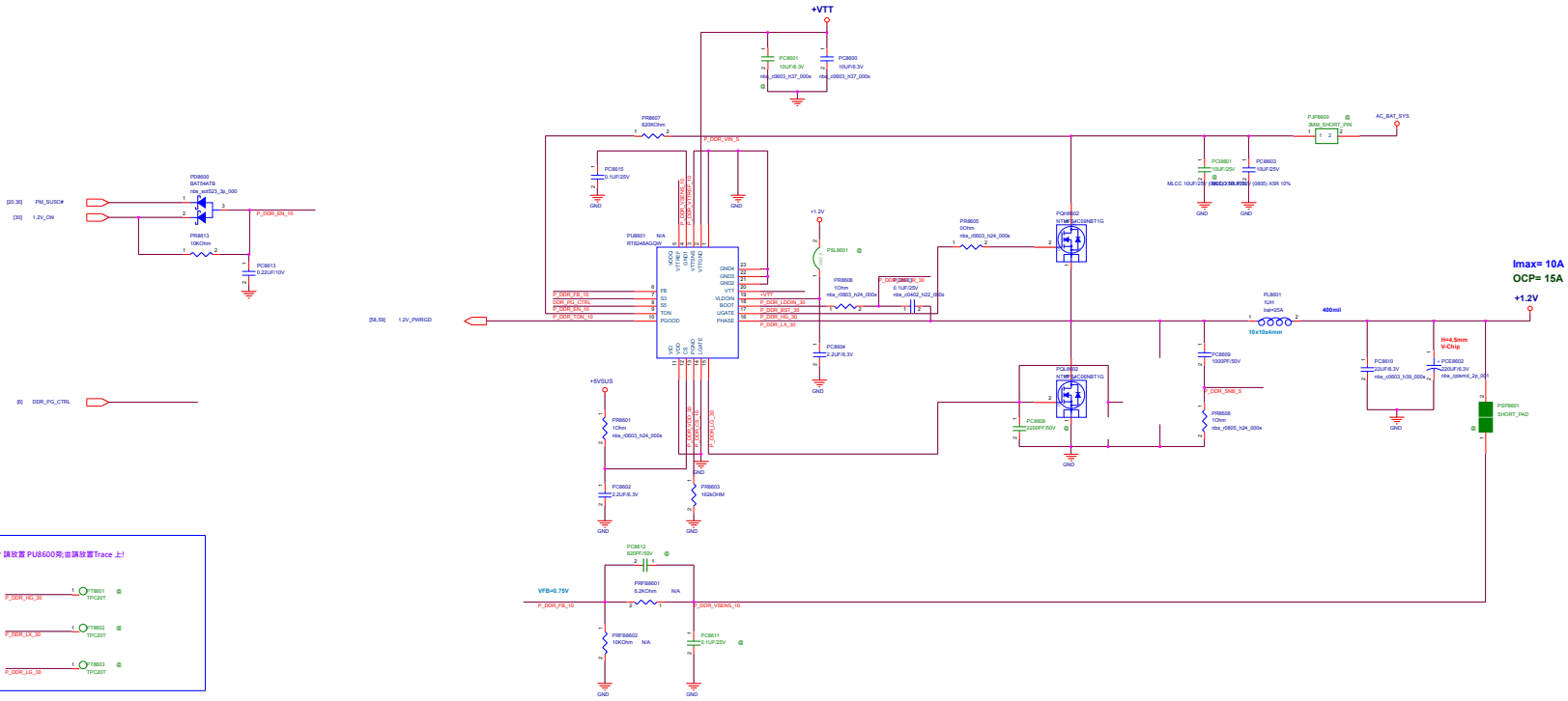
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		Project Name <b>G711GW</b>	Rev <b>R1.0</b>
<b>Title :</b> <b>PW_+1.0VSUS</b>			
Size <b>A3</b>	Dept.: <b>NB Power team</b>		Engineer: <b>Neil</b>
Date: <b>Tuesday, March 19, 2019</b>		Sheet <b>83</b> of <b>103</b>	



+1.2V / +VTT / +2.5V[For Memory]

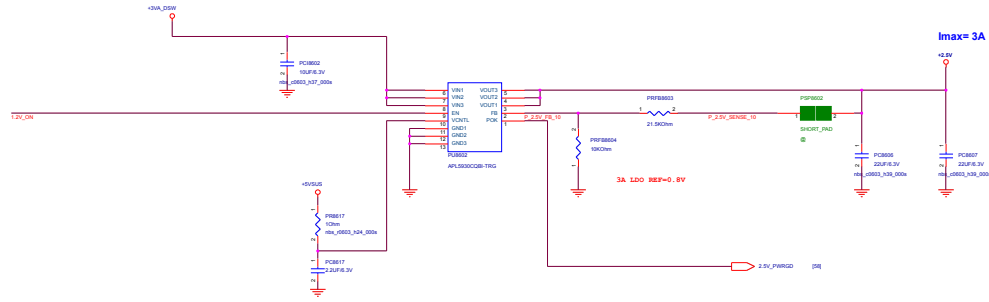


PT860\* 請放置 PU8600免,並請設置Trace上!

P10001 1 100nF 100nF

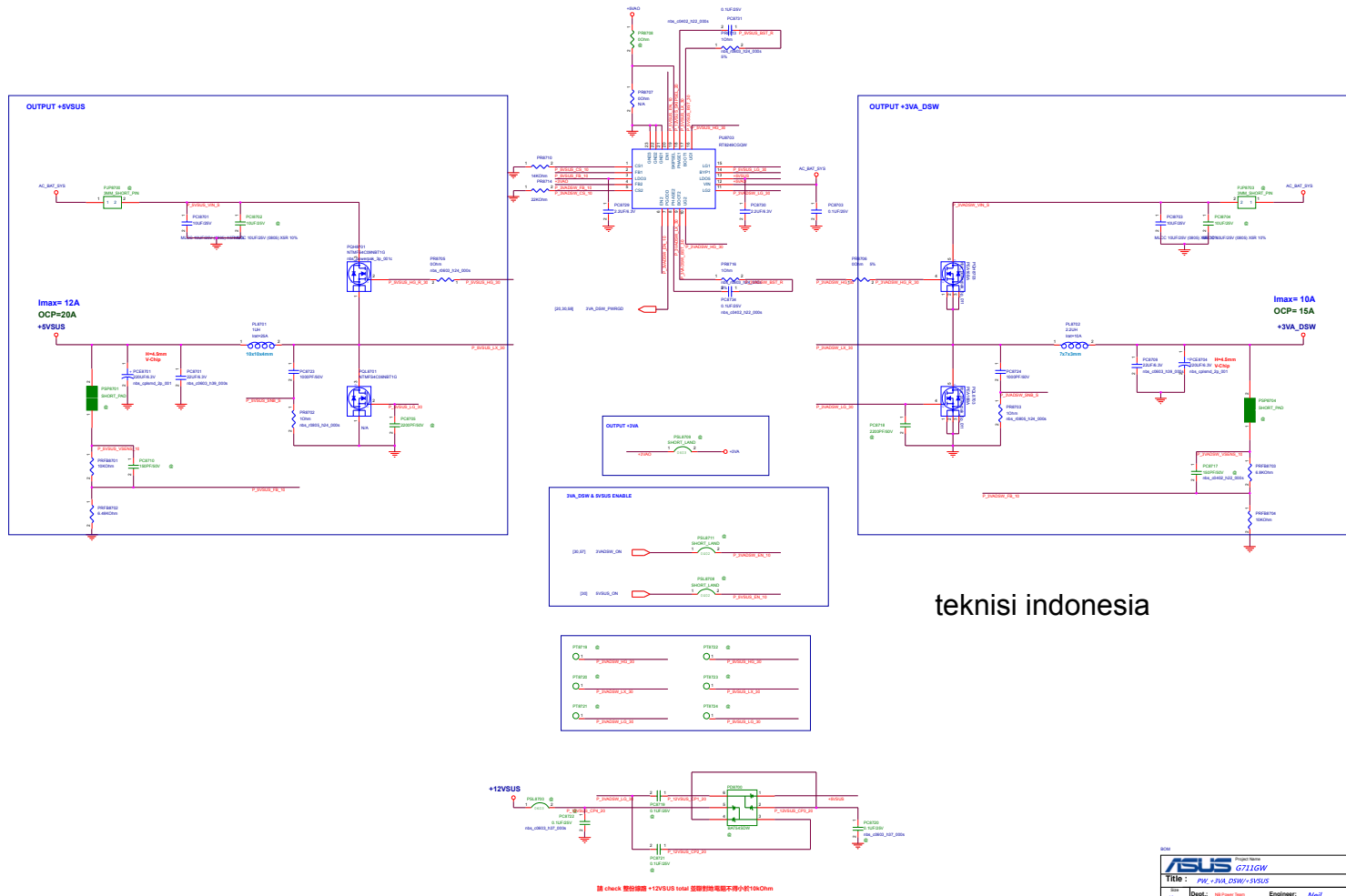
P10002 1 100nF 100nF

P10003 1 100nF 100nF



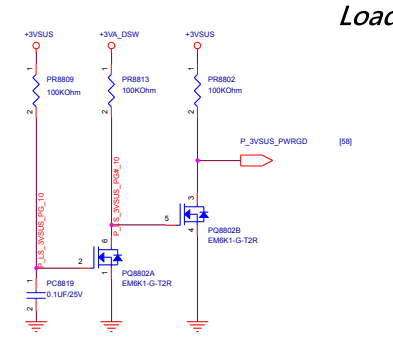
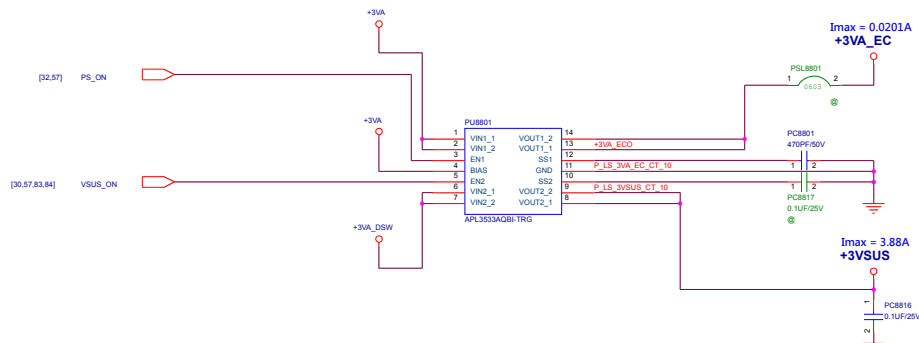


+3VA\_DSW / +5VSUS [System Power]



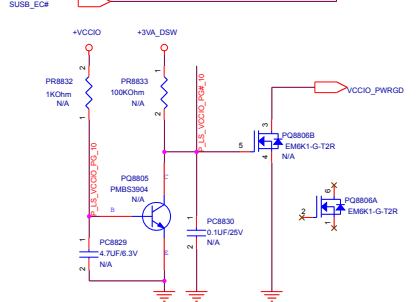
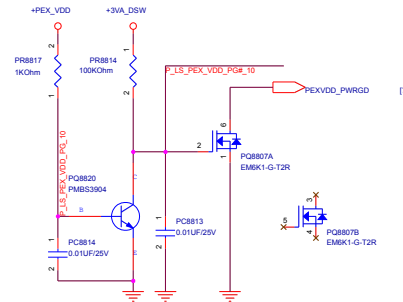
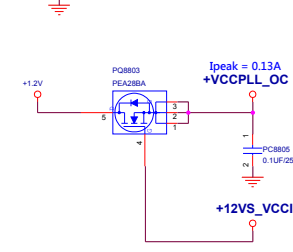
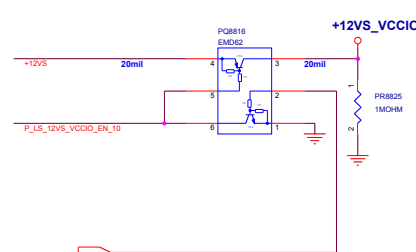
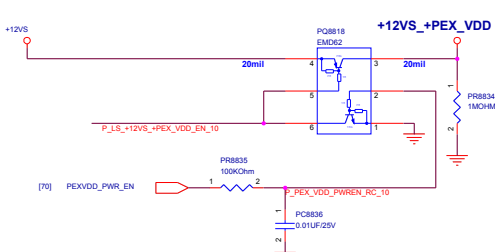
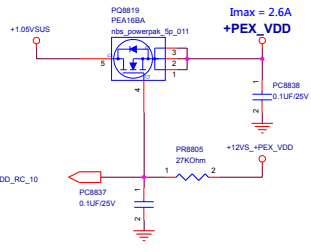
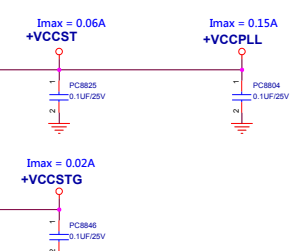
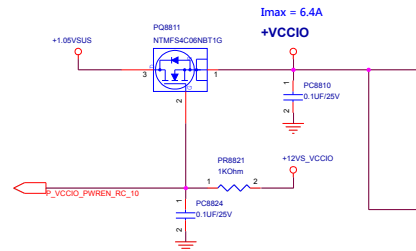
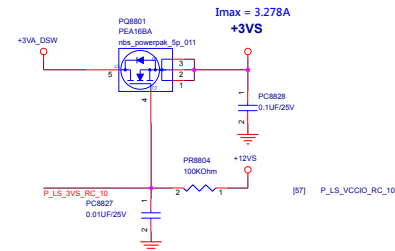
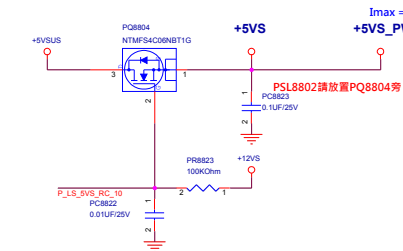
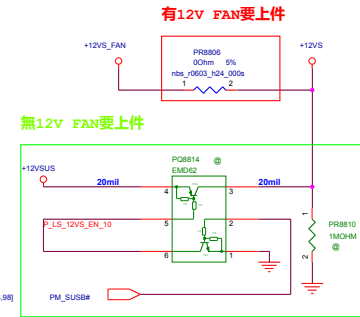
tekni Indonesia

ASUS G711GW		Rev
Title: PWR +3VA_DSW +5VSUS		41.0
Desig.	Rev	Engineer
Drawn	Checked	Printed



## Load Switch

Main Board

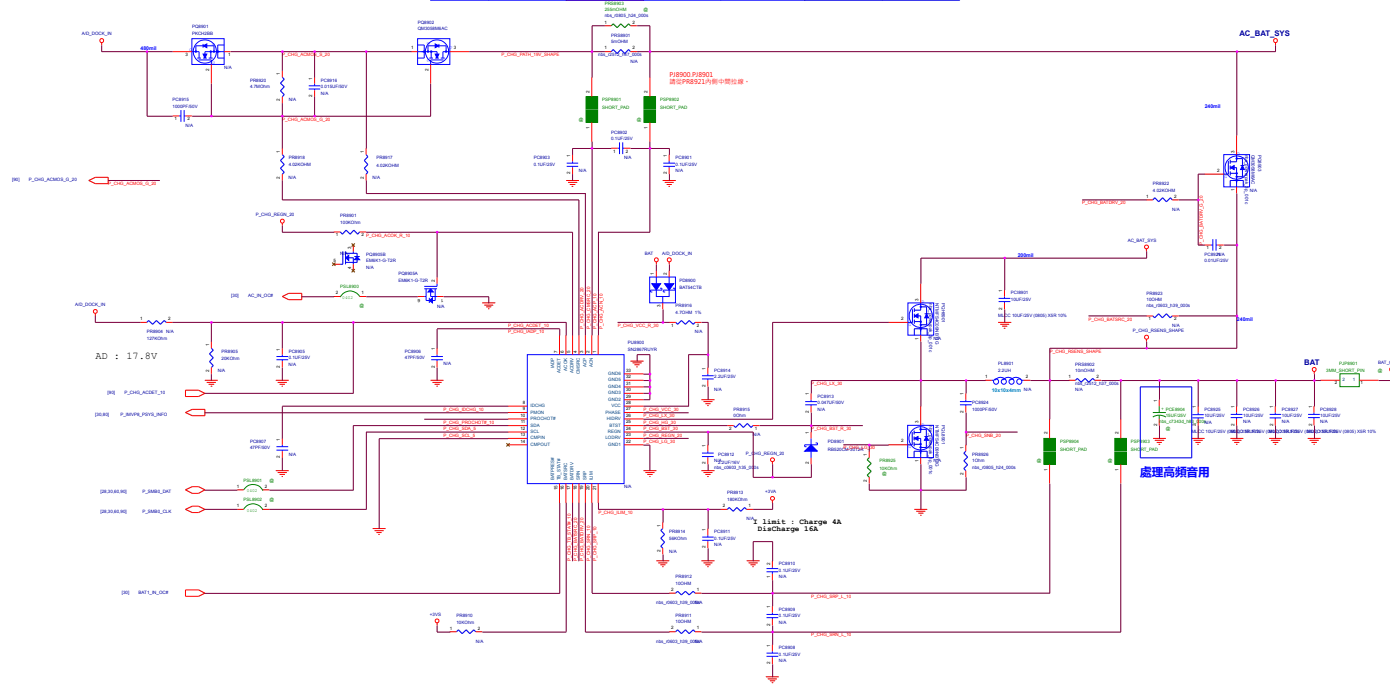


ASUS		Project Name	Rev
Coffeelake-H			R1.0
Title : PW_LOAD_SWITCH			
Size	Dept. : NS Power team	Engineer: Besnon	
A3	Date : Tuesday, March 10, 2019	Sheet 88	of 103

	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
YR8901	TBD	5m	5m	2m
YR8903	100K 1000000	100K 1000000	100K 1000000	100K 1000000

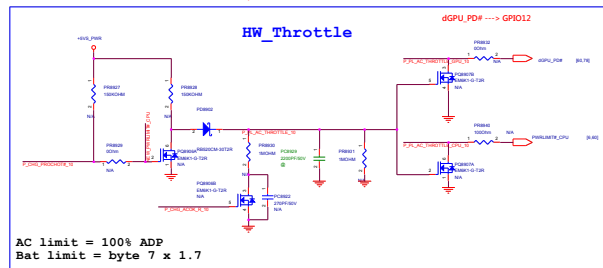
	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
YR8903	200m	255m	X	X	X	560m
	100K 1000000	100K 1000000	X	X	X	100K 1000000



Adaptor select  
total power = 90% ADP

HW\_Throttle

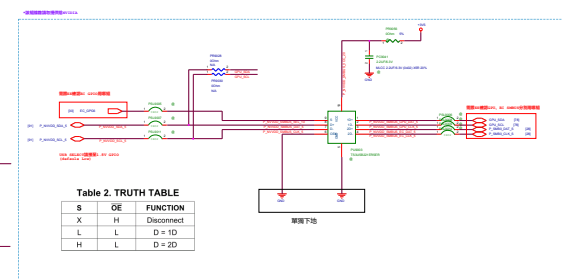
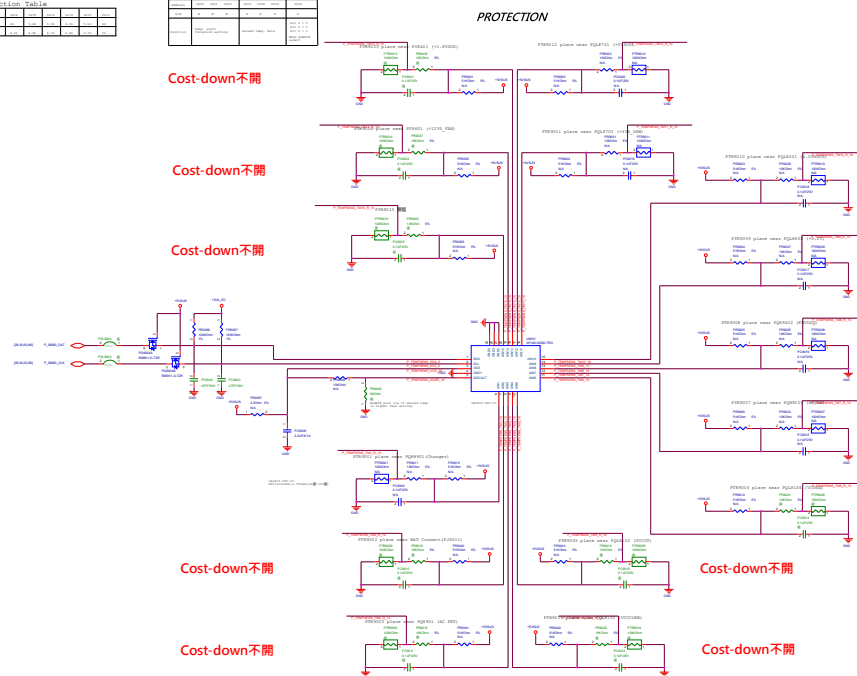
Adaptor select					
	N	Max	Min	Max	Min
PR8921	10m	5m			
PR8936					
14K	0.4V	30W	120W		
31.6K	0.8V	40W	150W		
56K	1.2V	45W	180W		
93.1K	1.6V	65W	230W		
150K	2.0V	75W	280W		
270K	2.4V	90W	330W		
560K	2.8V	120W	400W		



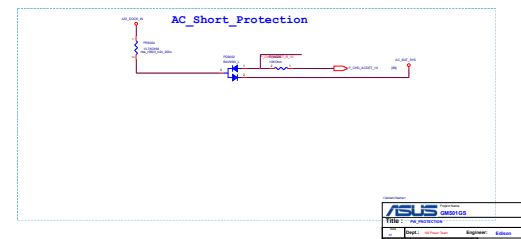
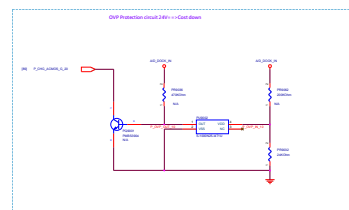
ASUS	Project Name	Rev
Coffee lake-R		Rev. 1
Title :	PW CHARGER	
Dept. :	AS Power Dept	Engineer : Benison
DATE :	2018/08/16	REV : 01

[illegible]

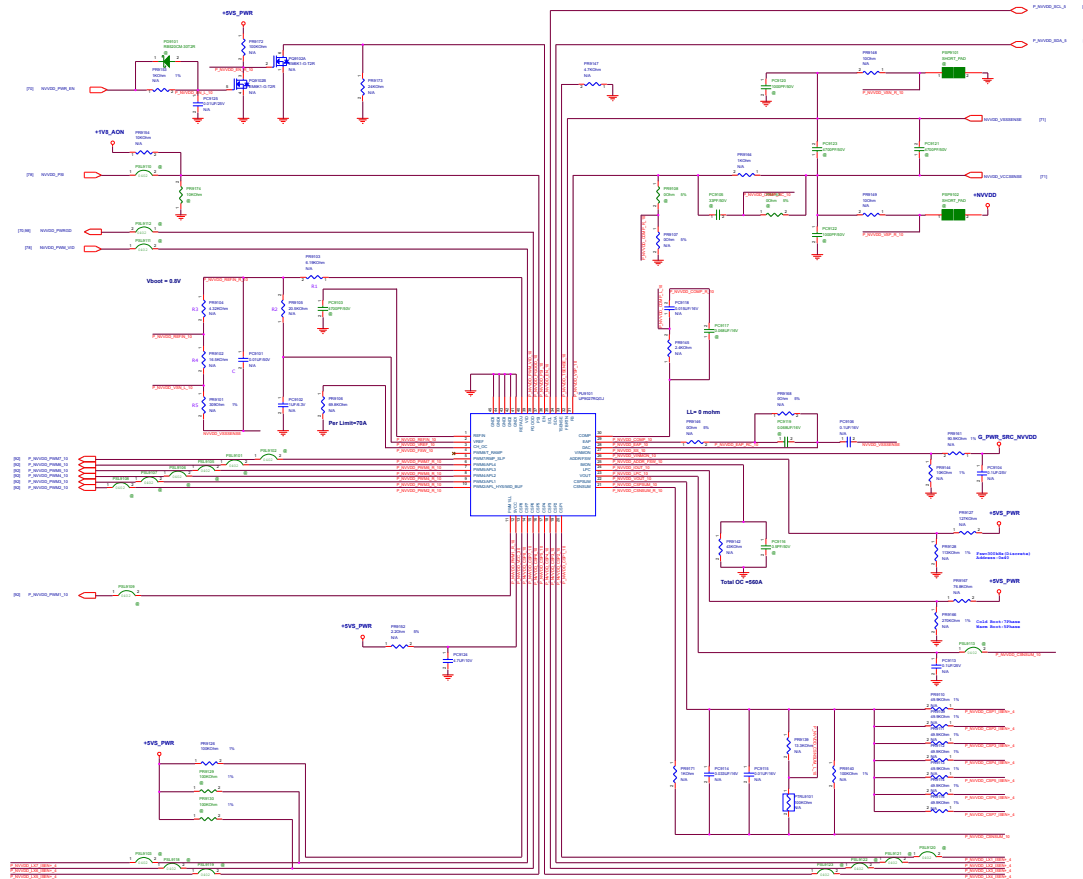
Register Address									
address	byte	byte	byte	byte	byte	byte	byte	byte	byte
0x0	0	0	0	0	0	0	0	0	0
function	temp, result threshold setting				lowest temp. data				000 0 0 0 000 0 0 0 000 0 0 0 000 0000



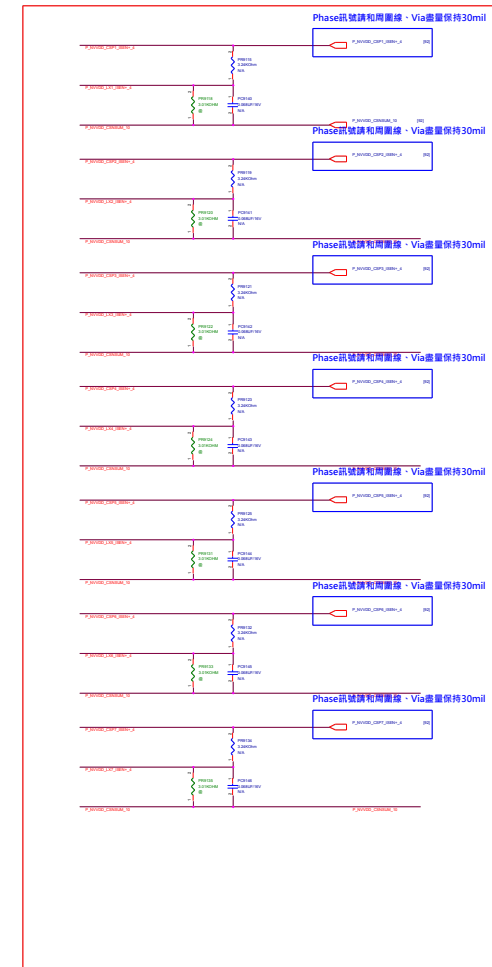
teknisi indonesia



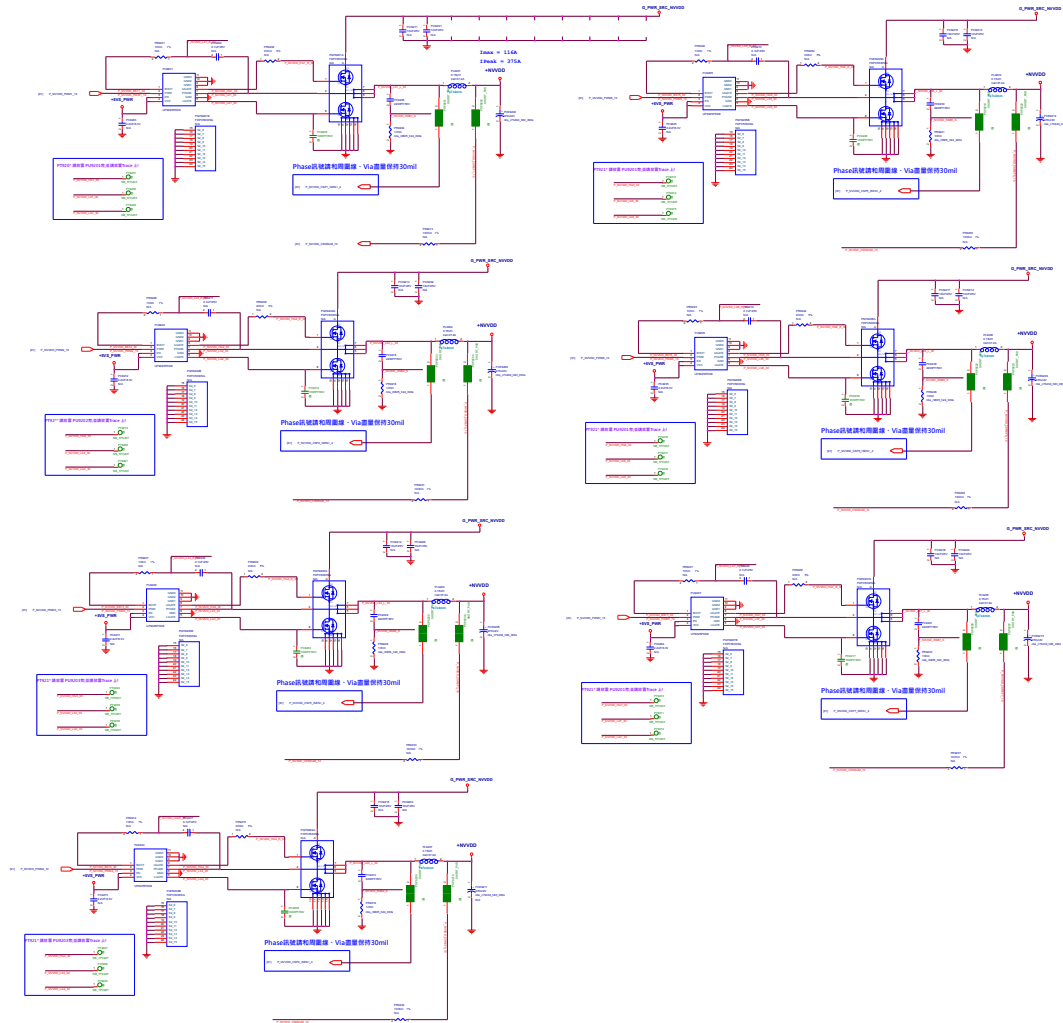
+NVVDD [For DGPU]



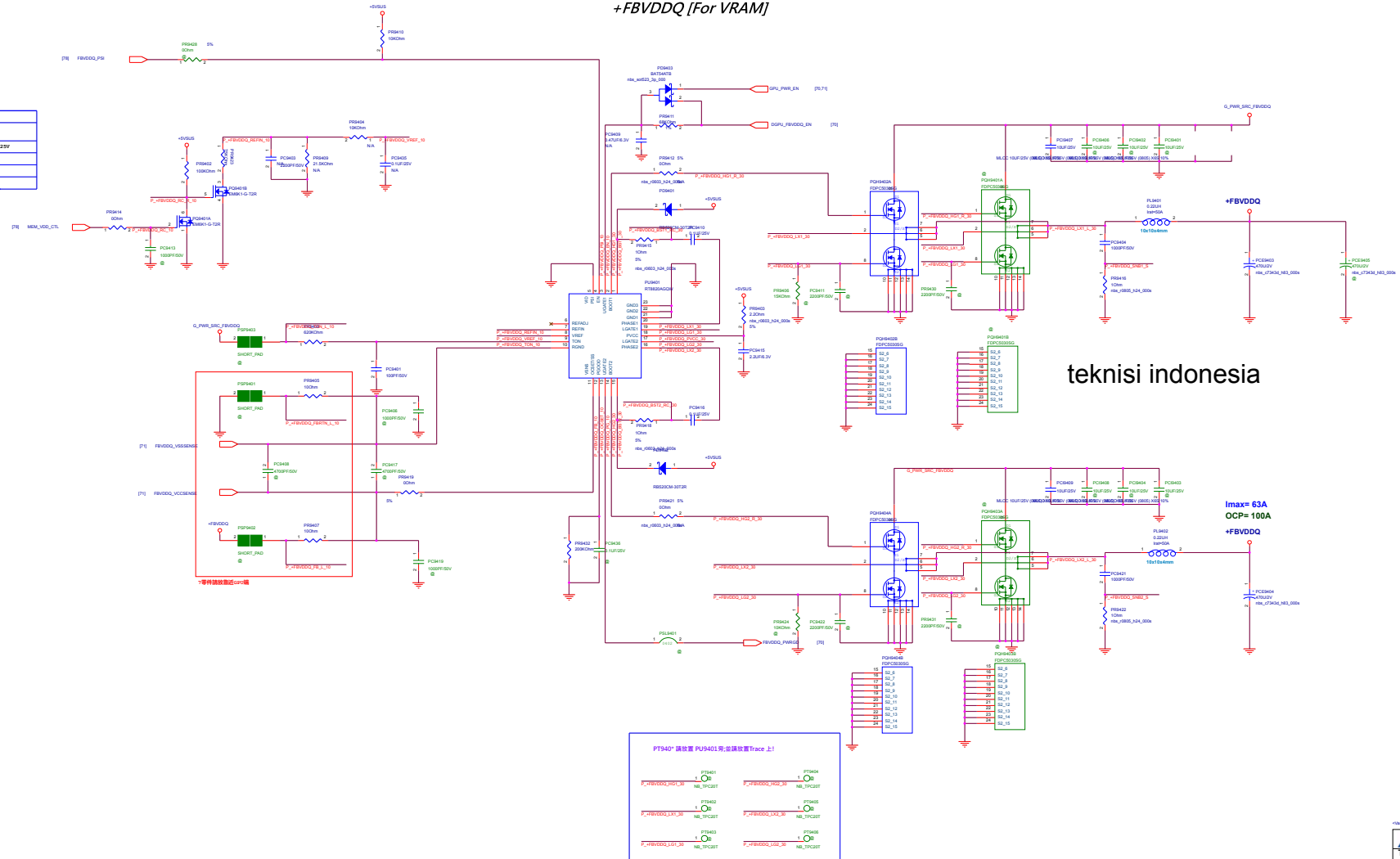
請放靠近PU9101



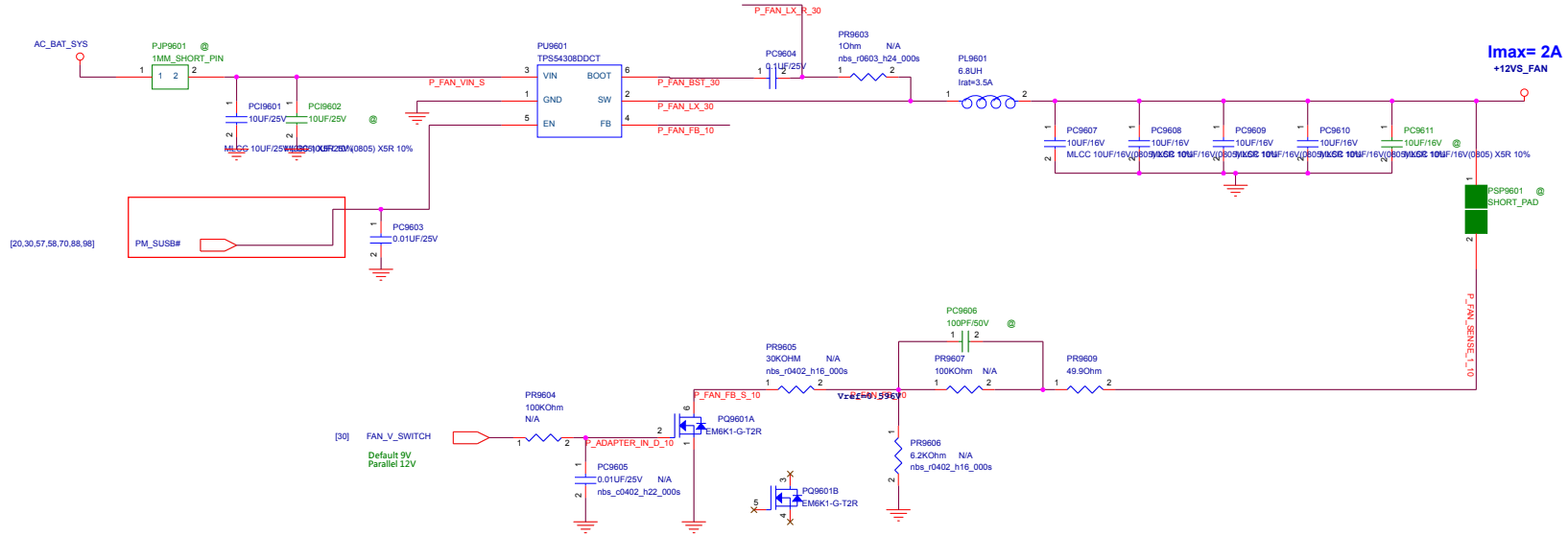
+NVVDD [For DGPU]




DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PS9404	5800nm	
PS9405	23.580nm	
PS9423	7580nm	



***+12VS\_FAN [For FAN]***

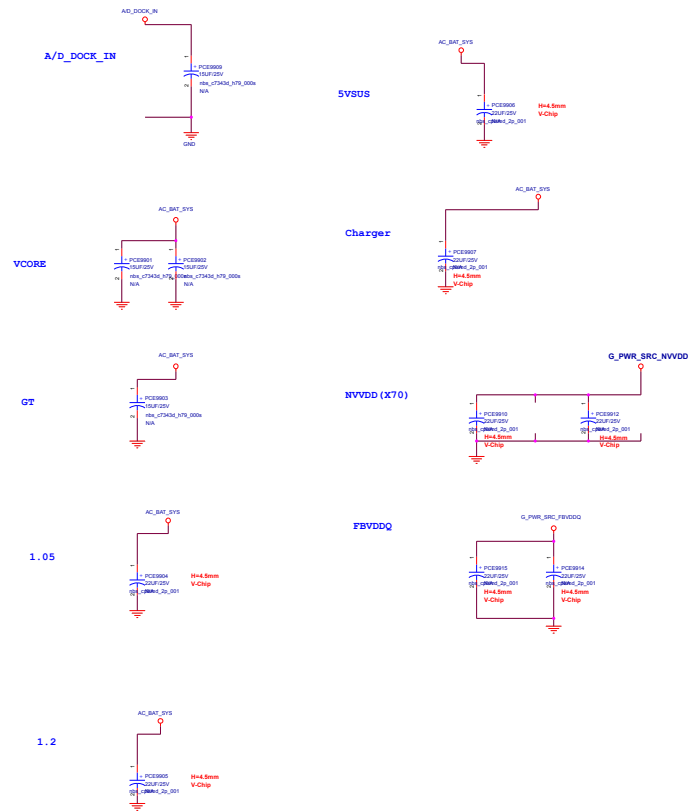


<Variant Name>

		Project Name		Rev
		Coffeelake-H		R1.0
<b>Title :</b> PW_*12VS_FAN				
Size	<b>Dept.:</b> NB Power team		<b>Engineer:</b> Hon	
B			Sheet	96 of 103
Date: Tuesday, March 19, 2019				





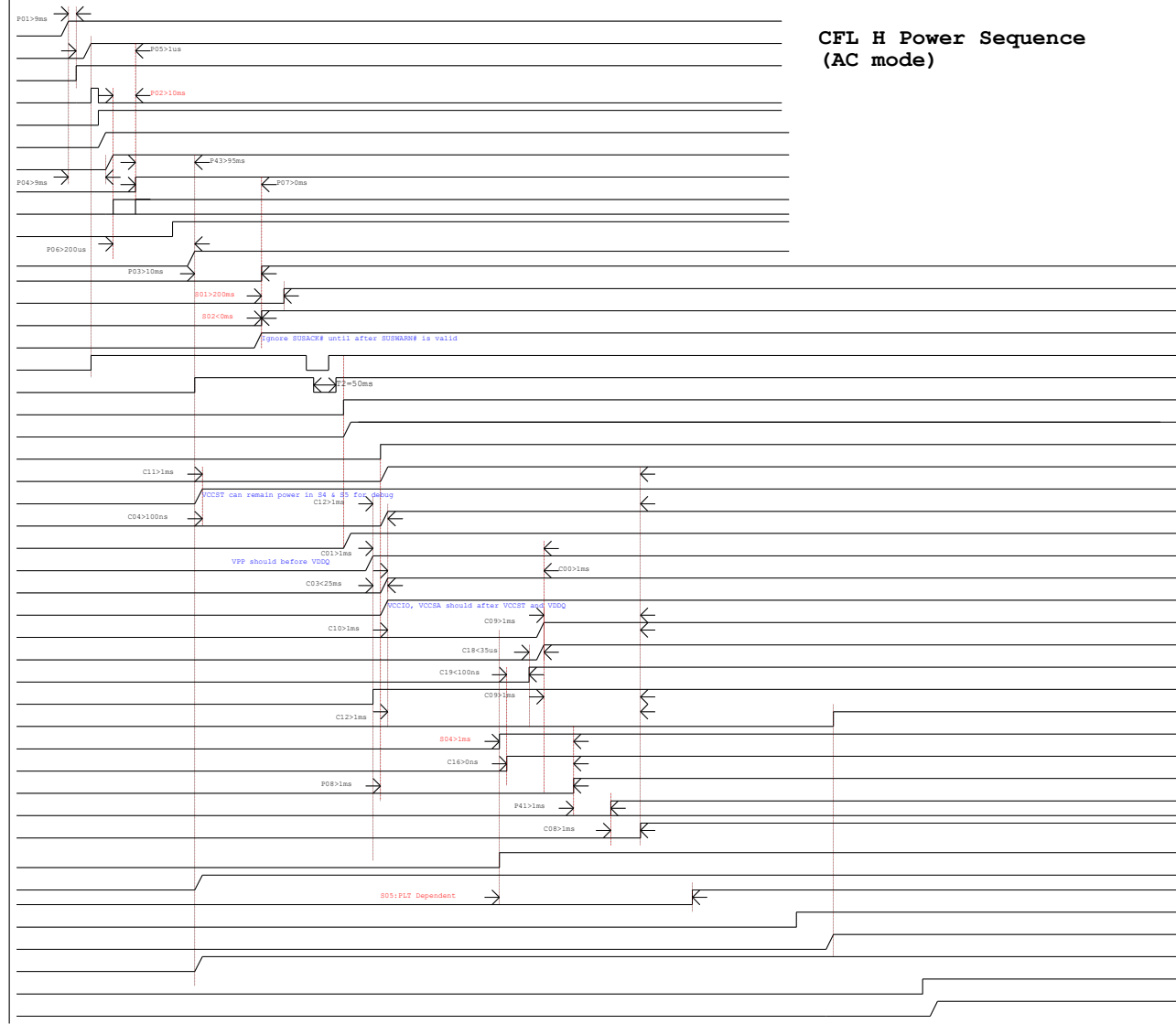


**\*共12顆**  
**\*請將對應電容放置對應PWR VRM輸入端**

Project Name		Rev
ASUS		B1.0
Title : PM_Input CAP		
Size	Dept. : Power Team	Engineer: Joe
Date : Thursday, March 15, 2018	Drawn : JB	of 100

## AC-IN Mode

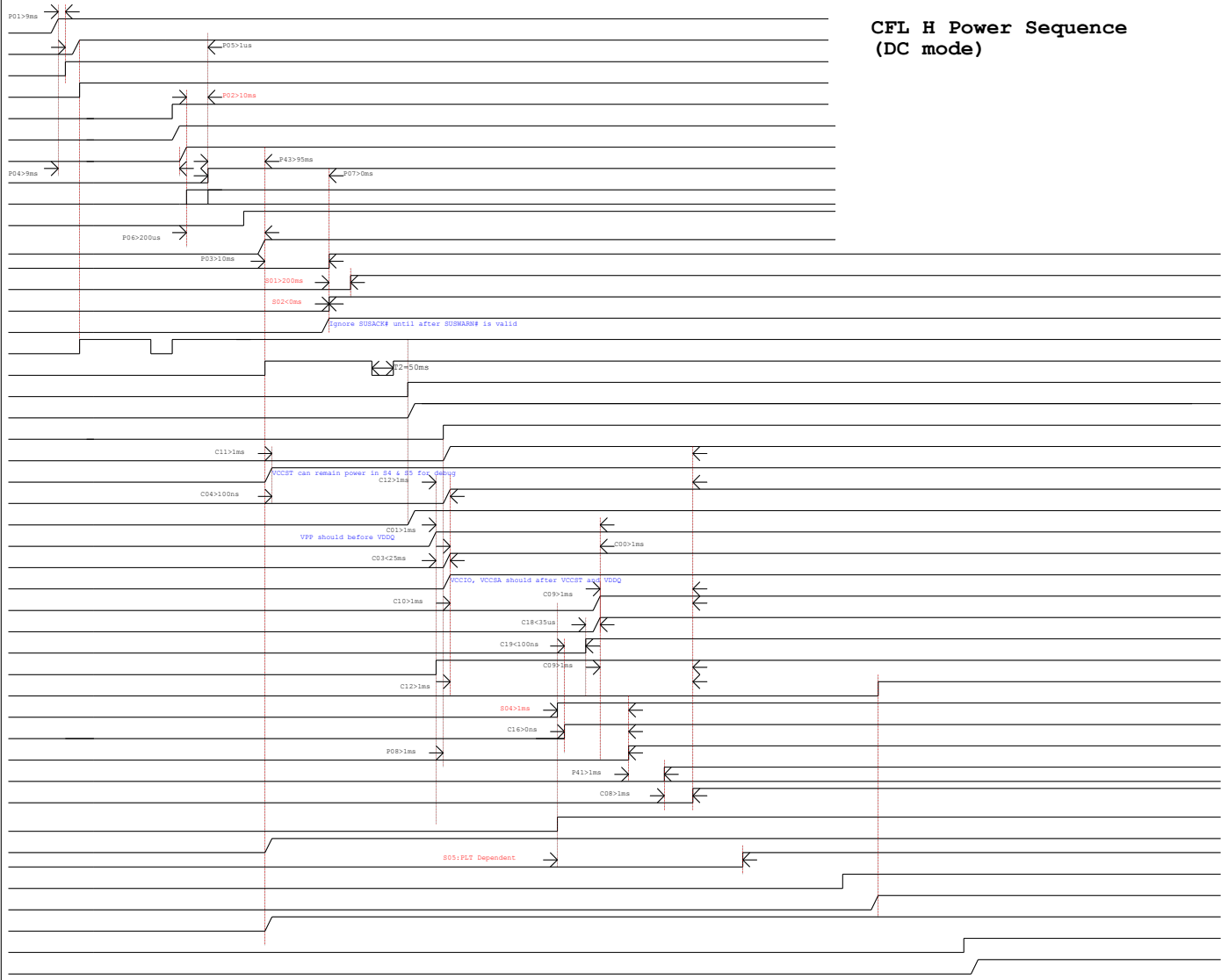
C:CPU (+RTCBAT)+3VA\_RTC  
P:PCH (AC\_BAT\_SYS)+3VA/+5VA  
S:PLT (+3VA\_RTC)RTCRST# (PCH)  
Power (Power)AC\_IN\_OC# (EC)  
Signal (EC)PS\_ON (+3VA\_EC)  
(PS\_ON)+3VA\_EC (EC)  
(3VADSW\_ON)+3VA\_DSW (3VA\_DSW\_PWRGD)  
(EC)DPWROK\_EC (PCH)  
(+3VA\_DSW)PM\_BATLOW# (PCH)  
(PCH)PM\_SLP\_SUS# (EC)  
(VSUS\_ON)+1.0VSUS\_VCCPRIM (1.0VSUS\_PWRGD)  
(EC)PM\_RSMRST#\_PCH (PCH)  
(PCH)SUSWARN# (EC)  
(EC)ME\_AC\_PRESENT\_PCH (PCH)  
(EC)PCH\_SUSACK# (PCH)  
(PWR Switch)PWR\_SW# (EC)  
(EC)PM\_PWRBTN# (PCH)  
(EC)SUSC\_EC# (Power)  
(SUSC\_EC#)+12V/+5V/+3V  
(EC)SUSB\_EC# (Power)  
(SUSB\_EC#)+12VS/+5VS/+3VS  
(SUSB\_EC#)+1.0V\_VCCST,VCCPLL  
(SUSB\_EC#)+VCCIO, (+12VS)+VCCSTG  
(1.2V\_ON)+2.5V (2.5V\_PWRGD)  
(1.2V\_ON)+VDDQ\_CPU (1.2V\_PWRGD)  
(+12VS)+VCCPLL\_OC  
(SUSB\_EC#)+VCCIO (VCCIO\_PWRGD)  
(ALL\_SYSTEM\_PWRGD)+VCCSA (IMVP8\_PWRGD)  
(DDR\_VTT\_CTRL)+0.6V  
(CPU)DDR\_VTT\_CTRL (Power)  
(Power)1.2V\_PWRGD (AND)  
(Power)IMVP8\_PWRGD  
(AND)ALL\_SYSTEM\_PWRGD (CPU/PCH/EC/Power)  
(ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU (CPU)  
(EC)PM\_PWROK\_PCH (PCH)  
(PCH)CLK\_PCH\_BCLK (CPU)  
(PCH)H\_CPU\_PWRGD (CPU)  
  
(CPU)P\_SVID\_DATA\_X2 (Power)  
(EC)PM\_SYSPWROK\_PCH (PCH)  
(PCH)PLT\_RST# (CPU/EC/Device)  
(P\_IMVP8\_DRVON)+VCCCORE (IMVP8\_PWRGD)  
(CPU)H\_THERMTrip# (PCH)  
(PCH)DDR4\_DRAMRST# (Memory)  
  
+VCCGT



## CFL H Power Sequence (AC mode)

DC-IN Mode

C:CPU (+RTCBAT)+3VA\_RTC  
P:PCH (AC\_BAT\_SYS)+3VA/+5VA  
S:PLT (+3VA\_RTC)RTCRST# (PCH)  
Power (Power)AC\_IN\_OC# (EC)  
Signal (EC)PS\_ON (+3VA\_EC)  
(PS\_ON)+3VA\_EC (EC)  
(3VADSW\_ON)+3VA\_DSW (3VA\_DSW\_PWRGD)  
(EC)DPWROR\_EC (PCH)  
(+3VA\_DSW)PM\_BATLOW# (PCH)  
(PCH)PM\_SLP\_SUS# (EC)  
(VSUS\_ON)+1.0VSUS\_VCCPRIM (1.0VSUS\_PWRGD)  
(EC)PM\_RSMRST#\_PCH (PCH)  
(PCH)SUSWARN# (EC)  
(EC)ME\_AC\_PRESENT\_PCH (PCH)  
(EC)PCH\_SUSACK# (PCH)  
(PWR Switch)PWR\_SW# (EC)  
(EC)PM\_PWRBTN# (PCH)  
(EC)SUSC\_EC# (Power)  
(SUSC\_EC#)+12V/+5V/+3V  
(EC)SUSB\_EC# (Power)  
(SUSB\_EC#)+12VS/+5VS/+3VS  
(VSUS\_ON)+1.0V\_VCCST,VCCPLL (VCCST\_PWRGD)  
(+VCCIO)+VCCSTG  
(1.2V\_ON)+2.5V (2.5V\_PWRGD)  
(1.2V\_ON)+VDDQ\_CPU (1.2V\_PWRGD)  
(+12VS)+VCCPLL\_OC  
(SUSB\_EC#)+VCCIO (VCCIO\_PWRGD)  
(ALL\_SYSTEM\_PWRGD)+VCCSA (IMVP8\_PWRGD)  
(DDR\_VTT\_CTRL)+0.6V  
(CPU)DDR\_VTT\_CTRL (Power)  
(Power)1.2V\_PWRGD (AND)  
(Power)IMVP8\_PWRGD  
(AND)ALL\_SYSTEM\_PWRGD (CPU/PCH/EC/Power)  
(ALL\_SYSTEM\_PWRGD)VCCST\_PWRGD\_CPU (CPU)  
(EC)PM\_PWROR\_PCH (PCH)  
(PCH)CLK\_PCH\_BCLK (CPU)  
(PCH)H\_CPU\_PWRGD (CPU)  
(ALL\_SYSTEM\_PWRGD)P\_IMVP8\_EN\_10 (Power)  
(CPU)P\_SVID\_DATA\_X2 (Power)  
(EC)PM\_SYSPWROR\_PCH (PCH)  
(PCH)PLT\_RST# (CPU/EC/Device)  
(P\_IMVP8\_DRVON)+VCCCORE (IMVP8\_PWRGD)  
(CPU)H\_THERMTRIP# (PCH)  
(PCH)DDR4\_DRAMRST# (Memory)  
+VCCGT



CFL H Power Sequence  
(DC mode)

ASUS		Project Name	Rev
G711GW			W1.0
Title : Power On Timing-DC mode			
Dept.	ASUS/NA COMPUTER	Engineer	Gaming RD
Date	Tuesday, March 10, 2015	Draw	101 of 105